

TABLE: SYSTEM POWER STATE

Gx State (System State)	Sx State (System State)	Mx State (System State)	SW Power	M Power	SUS Power	AMT Power	A Power	B Power	User Observation	Chipset
G0	S0	M0	ON	ON	ON	ON	ON	ON	System Operating	Full On
G1	S3	M3	ON	ON	ON	ON	ON	OFF	Standby	Suspend-to-RAM (STR)
		M-OFF	ON	ON	ON	OFF	ON	OFF	Standby with USB wake enabled	
	Deep S3	M-OFF	ON	ON	OFF	OFF	ON	OFF	Standby	Suspend-to-Disk (STD)
	S4	M3	ON	ON	ON	ON	OFF	OFF	Hibernation with RTC wakeup	
G2	Deep S4	M-OFF	ON	ON	OFF	OFF	OFF	OFF	Hibernation or Shutdown	Soft Off
	S5	M3	ON	ON	ON	ON	OFF	OFF		
	Deep S5	M-OFF	ON	ON	OFF	OFF	OFF	OFF		
G3	S5 EC OFF	M-OFF	OFF	OFF	OFF	OFF	OFF	OFF	No Power	Mechanical Off
	---	---	OFF	OFF	OFF	OFF	OFF	OFF		

Schematics Mark Definition

BOM Structure	BTO Item
@	Not assembled.
EMC@	Assembled. EMC related parts.
RF@	Assembled. RF related parts.
ME@	Assembled. ME related parts.
DCI@	Assembled. Intel debug related parts.
VRAM_M@ VRAM_S@ VRAM@	Assembled. VRAM related parts. depends on what kind of VRAM you use.
P52@ P72@	Assembled. depends on which project use.
PRxxx,PCxxx, PLxxx	PWR related parts. If @, not assembled.

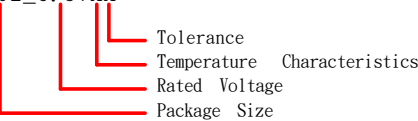
R0402 Short Footpirnt: R0402_SHORT
R0201 Short Footpirnt: R0201_SHORT

Any other mark like below is prohibited on Payton/Walter.
ESD@, EMI@, EMC_NS@, EMC_PX@, EMC_OPT@, CONN@,
CONN_NS@... RH, CH, LH(PCH related RLC)..

Capacitor Naming Note

Ceramic Capacitors:

0.1U_0402_6.3VXX



Temperature Characteristics:

Symbol	0	1	2	3	4	5	6	7	8	9	A
Code	Z5U	Z5V	Z5P	Y5U	Y5V	Y5P	X5R	X7R	NP0	COG	X6S

B	C	D	E	F	G	H	I	J	K	L
BJ	CH	CJ	CK	SH	SJ	UJ	UK	SL	X5S	NOJ

Tolerance:

Symbol	A	B	C	D	F	G	H	J	K	M	N
Tolerance	+0.05PF	+0.1PF	+0.25PF	+0.5PF	+1%	+2%	+3%	+5%	+10%	+20%	+30%

Symbol	P	Q	V	X	Z	S	Y
Tolerance	+100,-0%	+30,-10%	+20,-10%	+40,-20%	+80,-20%	+50,-20%	-30% ~ 10%

EC SMBus0 address

Device	Address
Smart Battery	0001 011X b

EC SMBus1 address

Device	Address
G-Senor (LIS3DH)	0011 000Xb
G-Senor (KX023)	0011 110Xb

EC SMBus2 address

Device	Address
Charge Controller	0001 0010

EC SMBus10 address

Device	Address
Master VGA	0x9E

PCH SM Bus address

Device	Address
CH-A P DDR DIMM0	1001 0000b
CH-A S DDR DIMM1	1001 0001b
CH-B P DDR DIMM2	1001 0010b
CH-B S DDR DIMM3	1001 0011b

PCH SM Bus0 address

Device	Address
Intel Lan_I219	0XC8

LC Future Center Secret Data

Project Name

Walter-3

Rev 0.5

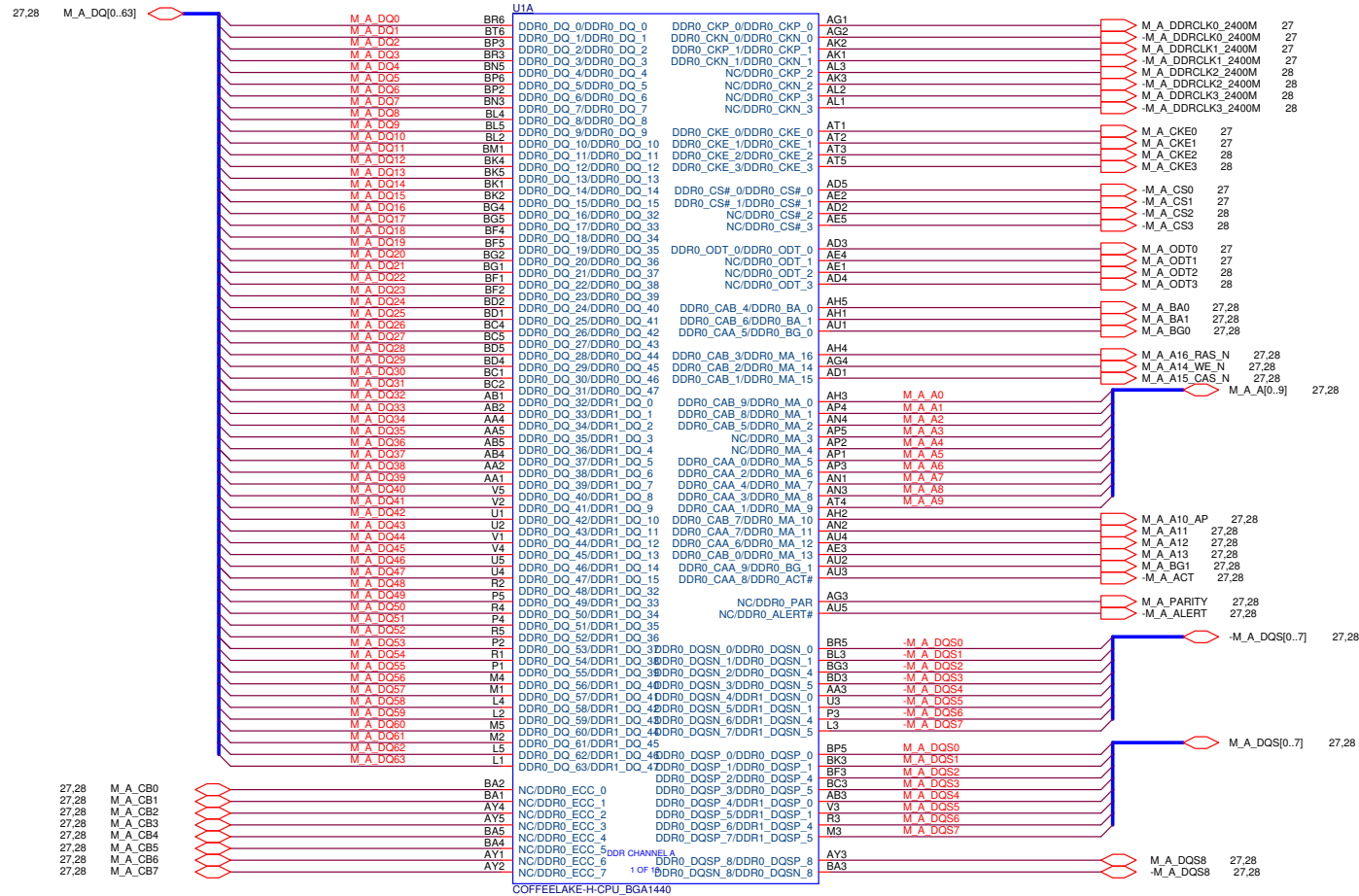
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EC HISTORY

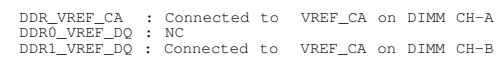
Date: Monday, June 25, 2018

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CPU

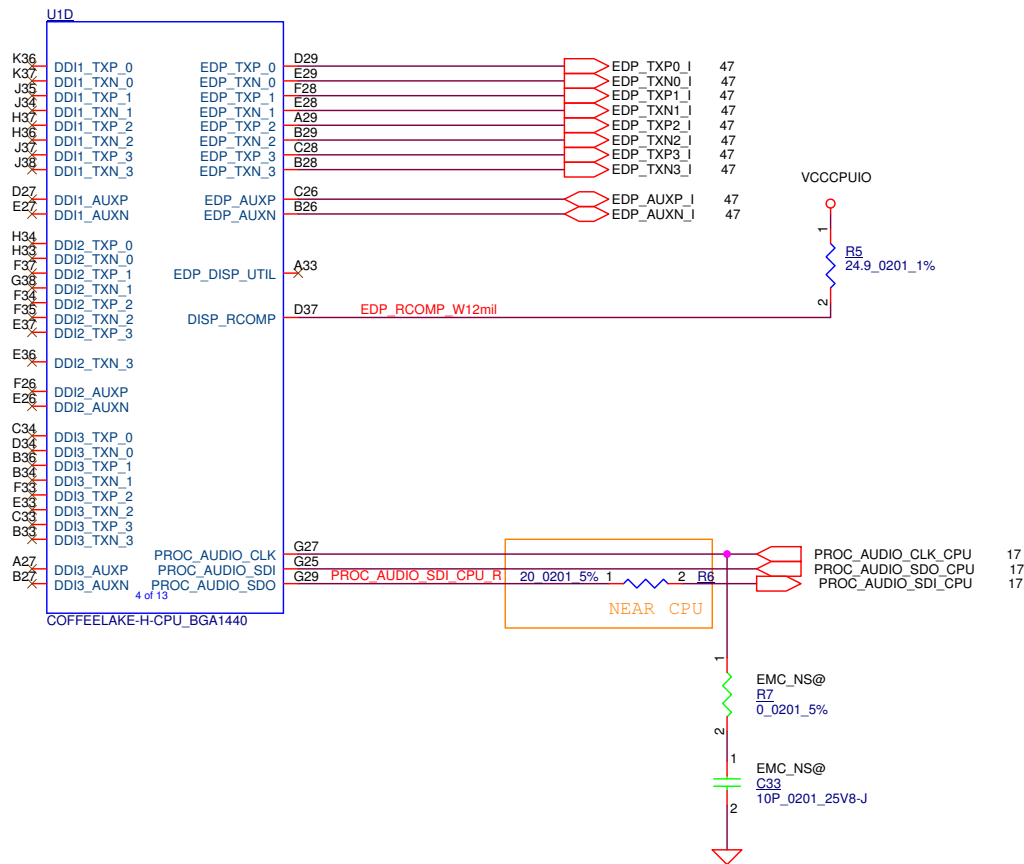


DDR4 INTERLEAVE IMPLEMENTATION

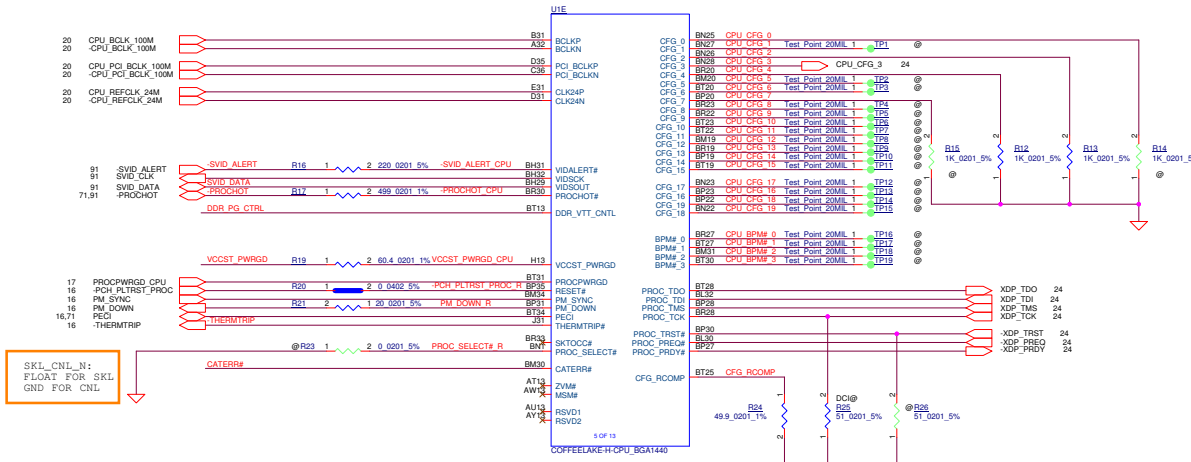
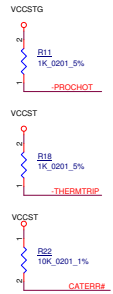
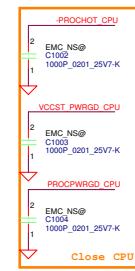
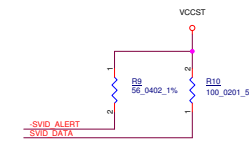
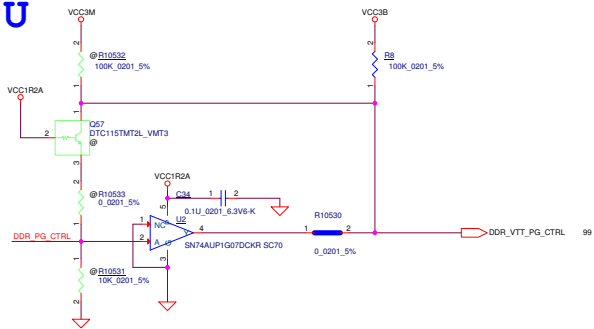


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CPU

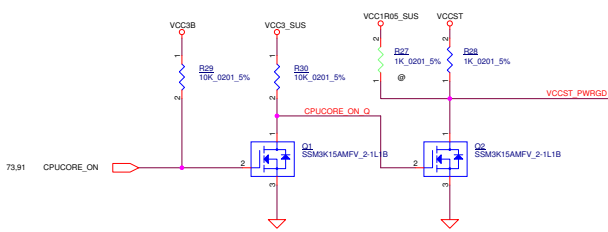


CPU



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If VCCSTG is used instead of VCC1R05_SUS, VCCSTG will be off in Sleep S0 because VCCSTG may be turned off when in Sleep S0. Currently, VCCSTG is still on in Sleep S0 but we may change logic to turn off VCCSTG in sleep S0. (CT_20141216)



VCCST_PWRGD requirements
1) Indication that the VCCST/VDDQ power supplies are stable and within specification
2) VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST
3) VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it.

TABLE CFG[19:0] pin has internal Pull up to VCCCPUIO with 5-8 k ohm.

CFG[0] : Stall reset sequence after CPU PLL lock until de-asserted:	
1 : No Stall	<----- LOGIC
0 : Stall	
CFG[2] : PEG Static Lane Reversal	
1 : Normal Operation	
0 : Lane Reversal	<----- LOGIC
CFG[4] : eDP enable	
1 : Disabled	
0 : Enabled	<----- LOGIC
CFG[6:5] : PEG Bifurcation, bus#:dev#:func#=0:1:0	
11 : 1x16	<----- LOGIC
CFG[7] : PEG Training	
1 : PEG Train immediately following RESET# deassertion	<----- LOGIC
0 : PEG Wait for BIOS for training	
CFG[19:8] : Reserved	
For x16 Reversal Lanes - CFG[6/5/2] setting is 110	
For x4 Reversal Lanes - CFG[6/5/2] setting is 000	

CPU

UIF		
A10	VSS_1	VSS_82
A12	VSS_2	VSS_83
A16	VSS_3	VSS_84
A18	VSS_4	VSS_85
A20	VSS_5	VSS_86
A22	VSS_6	VSS_87
A24	VSS_7	VSS_88
A26	VSS_8	VSS_89
A28	VSS_9	VSS_90
A30	VSS_10	VSS_91
A6	VSS_11	VSS_92
AA12	VSS_12	VSS_93
AA29	VSS_13	VSS_94
AA30	VSS_14	VSS_95
AB33	VSS_15	VSS_96
AB34	VSS_16	VSS_97
AB6	VSS_17	VSS_98
AC1	VSS_18	VSS_99
AC12	VSS_19	VSS_100
AC2	VSS_20	VSS_101
AC3	VSS_21	VSS_102
AC37	VSS_22	VSS_103
AC38	VSS_23	VSS_104
AC4	VSS_24	VSS_105
AC5	VSS_25	VSS_106
AC6	VSS_26	VSS_107
AD10	VSS_27	VSS_108
AD11	VSS_28	VSS_109
AD12	VSS_29	VSS_110
AD29	VSS_30	VSS_111
AD30	VSS_31	VSS_112
AD6	VSS_32	VSS_113
AD8	VSS_33	VSS_114
AD9	VSS_34	VSS_115
AE33	VSS_35	VSS_116
AE34	VSS_36	VSS_117
AE6	VSS_37	VSS_118
AF1	VSS_38	VSS_119
AF12	VSS_39	VSS_120
AF13	VSS_40	VSS_121
AF14	VSS_41	VSS_122
AF2	VSS_42	VSS_123
AF3	VSS_43	VSS_124
AF4	VSS_44	VSS_125
AG10	VSS_45	VSS_126
AG11	VSS_46	VSS_127
AG13	VSS_47	VSS_128
AG29	VSS_48	VSS_129
AG30	VSS_49	VSS_130
AG6	VSS_50	VSS_131
AG7	VSS_51	VSS_132
AG8	VSS_52	VSS_133
AH12	VSS_53	VSS_134
AH33	VSS_54	VSS_135
AH34	VSS_55	VSS_136
AH35	VSS_56	VSS_137
AH36	VSS_57	VSS_138
AH6	VSS_58	VSS_139
AJ1	VSS_59	VSS_140
AJ13	VSS_60	VSS_141
AJ2	VSS_61	VSS_142
AJ3	VSS_62	VSS_143
AJ37	VSS_63	VSS_144
AJ38	VSS_64	VSS_145
AJ4	VSS_65	VSS_146
AJ5	VSS_66	VSS_147
AJ6	VSS_67	VSS_148
W4	VSS_68	VSS_149
W5	VSS_69	VSS_150
Y10	VSS_70	VSS_151
Y11	VSS_71	VSS_152
Y13	VSS_72	VSS_153
Y14	VSS_73	VSS_154
Y37	VSS_74	VSS_155
Y38	VSS_75	VSS_156
Y7	VSS_76	VSS_157
Y8	VSS_77	VSS_158
Y9	VSS_78	VSS_159
AK29	VSS_79	VSS_160
AK30	VSS_80	VSS_161
AK30	VSS_81	VSS_162

COFFEE LAKE-H-CPU_BGA1440



UIH		
AW5	VSS_163	VSS_244
AY12	VSS_164	VSS_245
AY33	VSS_165	VSS_246
AY34	VSS_166	VSS_247
B9	VSS_167	VSS_248
BA10	VSS_168	VSS_249
BA11	VSS_169	VSS_250
BA12	VSS_170	VSS_251
BA37	VSS_171	VSS_252
BA38	VSS_172	VSS_253
BA6	VSS_173	VSS_254
BA7	VSS_174	VSS_255
BA8	VSS_175	VSS_256
BA9	VSS_176	VSS_257
BB1	VSS_177	VSS_258
BB12	VSS_178	VSS_259
BB2	VSS_179	VSS_260
BB29	VSS_180	VSS_261
BB3	VSS_181	VSS_262
BB30	VSS_182	VSS_263
BB4	VSS_183	VSS_264
BB5	VSS_184	VSS_265
BB6	VSS_185	VSS_266
BC12	VSS_186	VSS_267
BC13	VSS_187	VSS_268
BC14	VSS_188	VSS_269
BC33	VSS_189	VSS_270
BC34	VSS_190	VSS_271
BC6	VSS_191	VSS_272
BD10	VSS_192	VSS_273
BD11	VSS_193	VSS_274
BD12	VSS_194	VSS_275
BD37	VSS_195	VSS_276
BD6	VSS_196	VSS_277
BD7	VSS_197	VSS_278
BD8	VSS_198	VSS_279
BD9	VSS_199	VSS_280
BE1	VSS_200	VSS_281
BE2	VSS_201	VSS_282
BE29	VSS_202	VSS_283
BE3	VSS_203	VSS_284
BE30	VSS_204	VSS_285
BE4	VSS_205	VSS_286
BE5	VSS_206	VSS_287
BE6	VSS_207	VSS_288
BF12	VSS_208	VSS_289
BF33	VSS_209	VSS_290
BF34	VSS_210	VSS_291
BF6	VSS_211	VSS_292
BG12	VSS_212	VSS_293
BG13	VSS_213	VSS_294
BG14	VSS_214	VSS_295
BG37	VSS_215	VSS_296
BG38	VSS_216	VSS_297
BG6	VSS_217	VSS_298
BH1	VSS_218	VSS_299
BH10	VSS_219	VSS_300
BH11	VSS_220	VSS_301
BH12	VSS_221	VSS_302
BH14	VSS_222	VSS_303
BH2	VSS_223	VSS_304
BH3	VSS_224	VSS_305
BH4	VSS_225	VSS_306
BH5	VSS_226	VSS_307
BH6	VSS_227	VSS_308
BH7	VSS_228	VSS_309
BH8	VSS_229	VSS_310
BH9	VSS_230	VSS_311
T2	VSS_231	VSS_312
T3	VSS_232	VSS_313
T33	VSS_233	VSS_314
T34	VSS_234	VSS_315
T4	VSS_235	VSS_316
T5	VSS_236	VSS_317
T7	VSS_237	VSS_318
T8	VSS_238	VSS_319
T9	VSS_239	VSS_320
U37	VSS_240	VSS_321
U38	VSS_241	VSS_322
U39	VSS_242	VSS_323
U38	VSS_243	VSS_324
BU12	VSS_244	VSS_325
BU14	VSS_245	VSS_326

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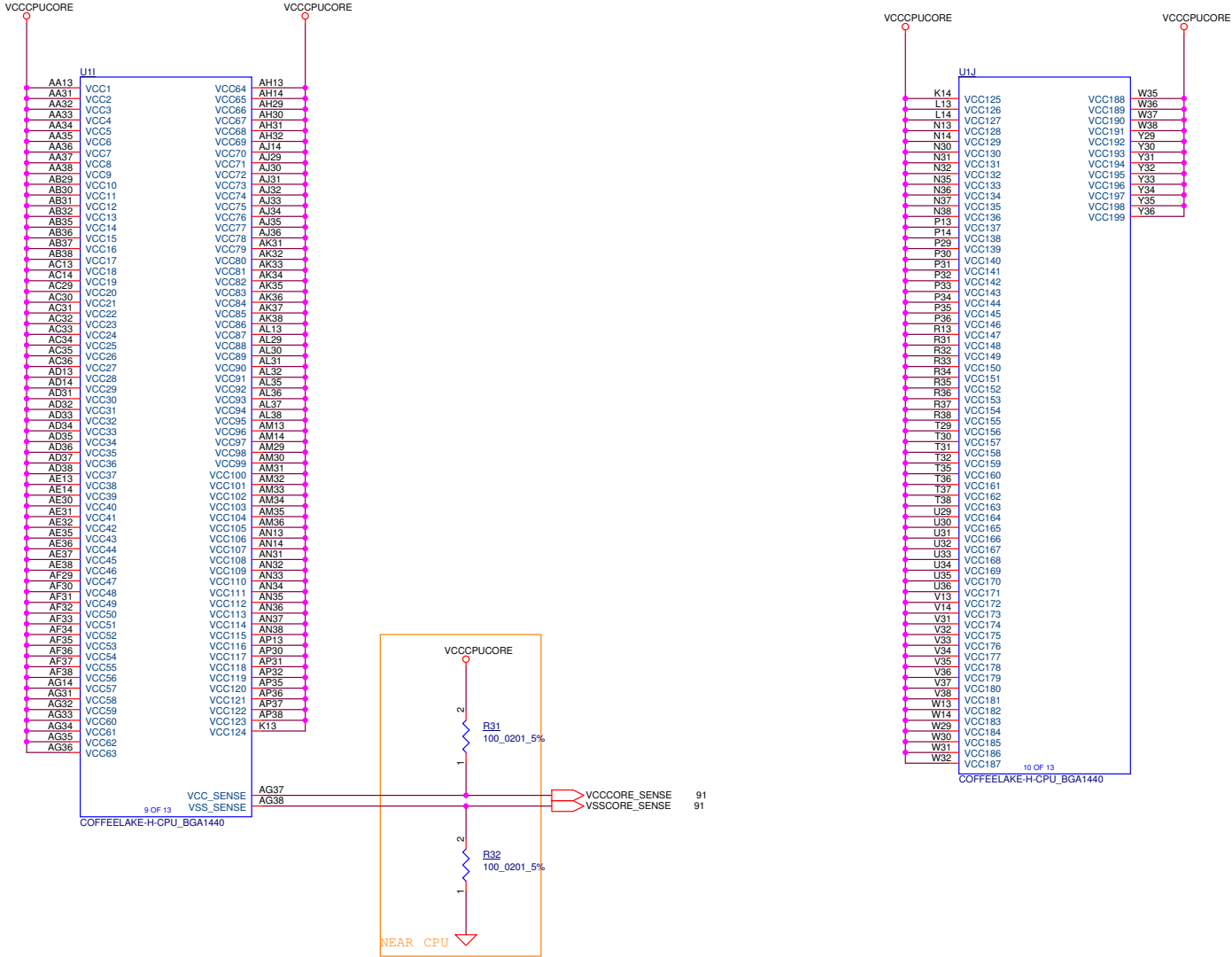
UIH		
BM4	VSS_325	VSS_409
BM7	VSS_326	VSS_410
BP12	VSS_327	VSS_411
BP14	VSS_328	VSS_412
BP18	VSS_329	VSS_413
BP21	VSS_330	VSS_414
BP24	VSS_331	VSS_415
BP26	VSS_332	VSS_416
BP29	VSS_333	VSS_417
BP33	VSS_334	VSS_418
BP34	VSS_335	VSS_419
BP7	VSS_336	VSS_420
BR12	VSS_337	VSS_421
BR14	VSS_338	VSS_422
BR18	VSS_339	VSS_423
BR21	VSS_340	VSS_424
BR24	VSS_341	VSS_425
BR25	VSS_342	VSS_426
BR26	VSS_343	VSS_427
BR29	VSS_344	VSS_428
BR34	VSS_345	VSS_429
BR36	VSS_346	VSS_430
BR7	VSS_347	VSS_431
BT12	VSS_348	VSS_432
BT14	VSS_349	VSS_433
BT18	VSS_350	VSS_434
BT21	VSS_351	VSS_435
BT24	VSS_352	VSS_436
BT26	VSS_353	VSS_437
BT29	VSS_354	VSS_438
BT32	VSS_355	VSS_439
BT5	VSS_356	VSS_440
C11	VSS_357	VSS_441
C13	VSS_358	VSS_442
C15	VSS_359	VSS_443
C17	VSS_360	VSS_444
C19	VSS_361	VSS_445
C21	VSS_362	VSS_446
C23	VSS_363	VSS_447
C25	VSS_364	VSS_448
C27	VSS_365	VSS_449
C29	VSS_366	VSS_450
C31	VSS_367	VSS_451
C37	VSS_368	VSS_452
C5	VSS_369	VSS_453
C8	VSS_370	VSS_454
C9	VSS_371	VSS_455
D10	VSS_372	VSS_456
D12	VSS_373	VSS_457
D14	VSS_374	VSS_458
D16	VSS_375	VSS_459
D18	VSS_376	VSS_460
D19	VSS_377	VSS_461
D20	VSS_378	VSS_462
D22	VSS_379	VSS_463
D24	VSS_380	VSS_464
D26	VSS_381	VSS_465
D28	VSS_382	VSS_466
D3	VSS_383	VSS_467
D30	VSS_384	VSS_468
D33	VSS_385	VSS_469
D6	VSS_386	VSS_470
D9	VSS_387	VSS_471
E34	VSS_388	VSS_472
E35	VSS_389	VSS_473
E38	VSS_390	VSS_474
E4	VSS_391	VSS_475
E9	VSS_392	VSS_476
N3	VSS_393	VSS_477
N33	VSS_394	VSS_478
N34	VSS_395	VSS_479
N4	VSS_396	VSS_480
N5	VSS_397	VSS_481
N6	VSS_398	VSS_482
N7	VSS_399	VSS_483
N8	VSS_400	VSS_484
N9	VSS_401	VSS_485
P12	VSS_402	VSS_486
P37	VSS_403	VSS_487
M14	VSS_404	VSS_488
M6	VSS_405	VSS_489
N1	VSS_406	VSS_490
F11	VSS_407	VSS_491
F13	VSS_408	VSS_492

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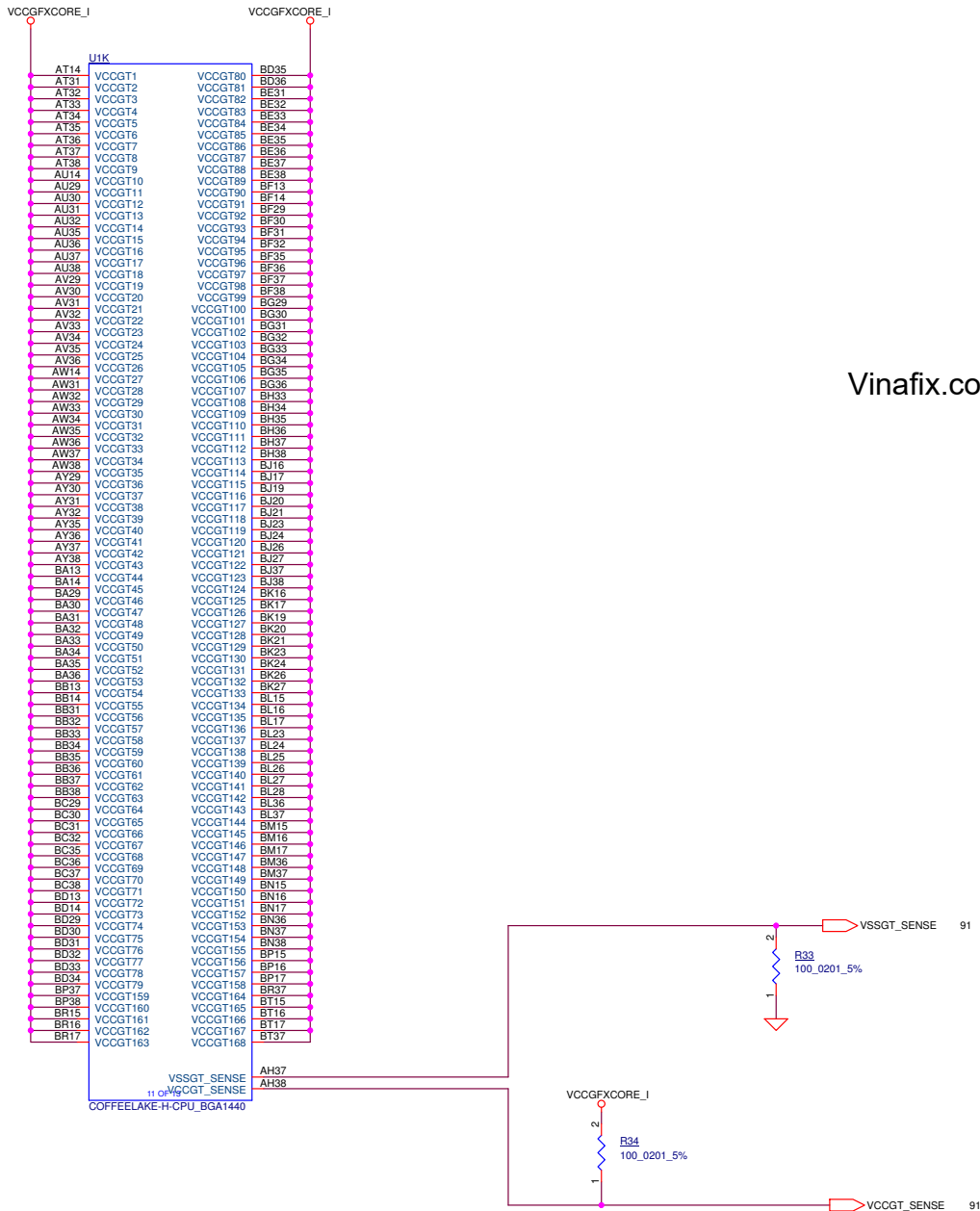


CPU NCTF UR 1	Test Point 20MIL 1	TP65	@
CPU NCTF LR 2	Test Point 20MIL 1	TP67	@
CPU NCTF UR 2	Test Point 20MIL 1	TP66	@
CPU NCTF LR 1	Test Point 20MIL 1	TP68	@

CPU

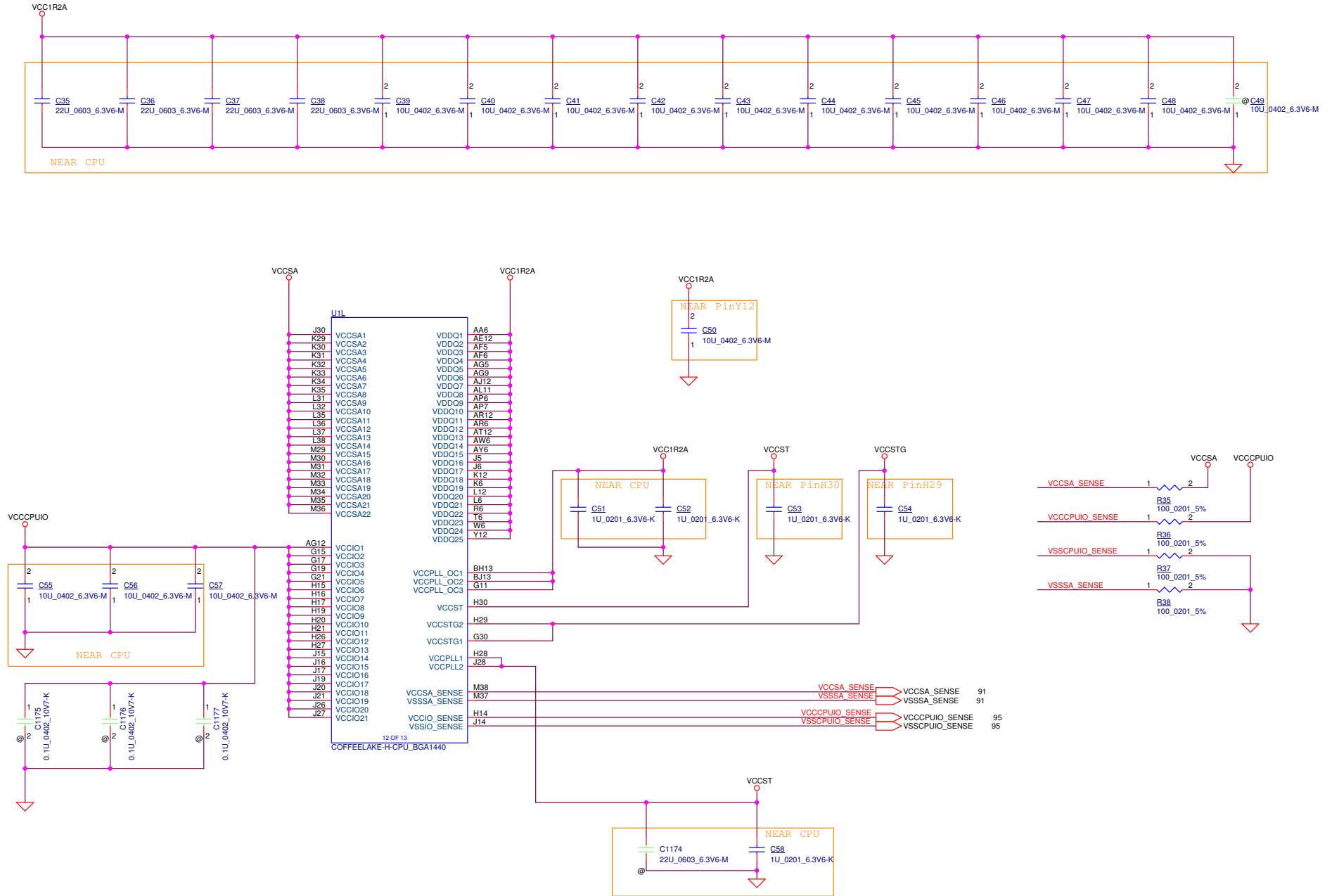


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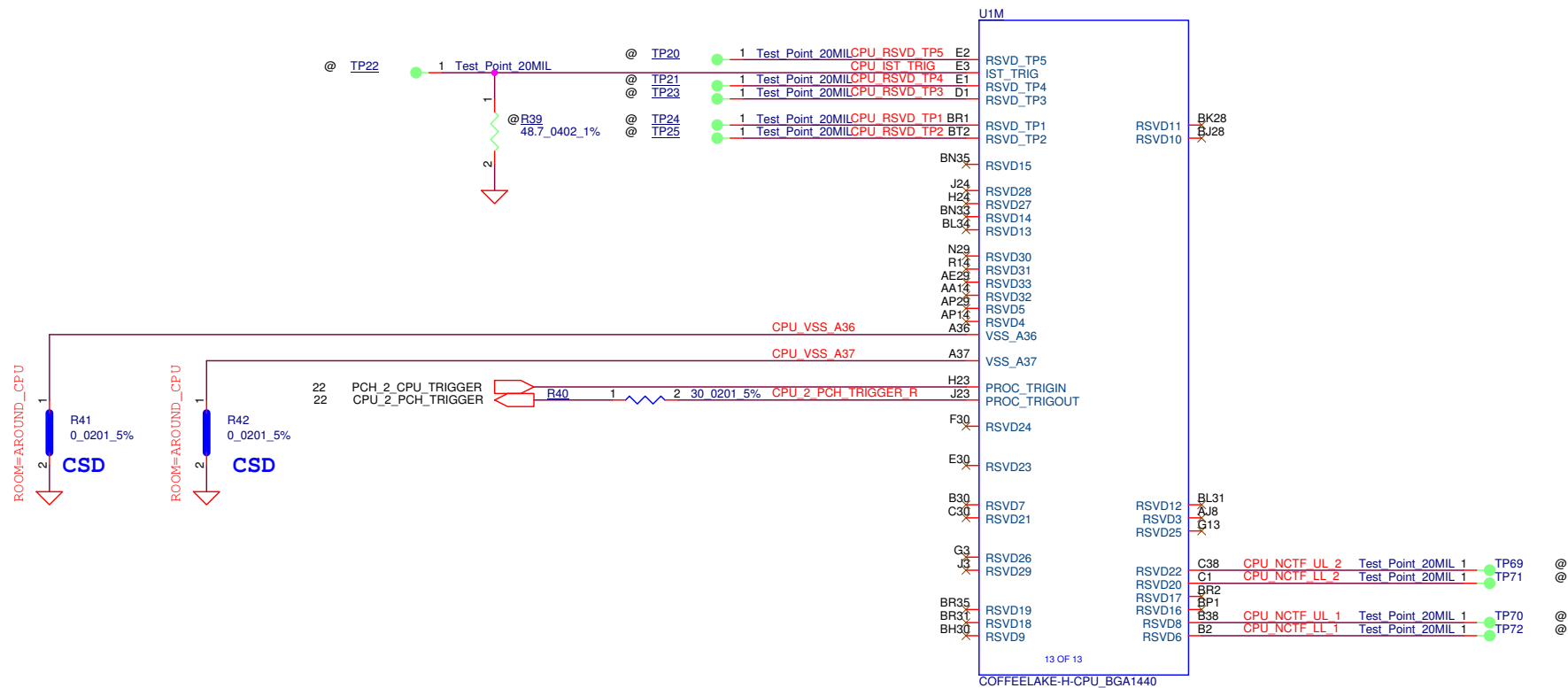


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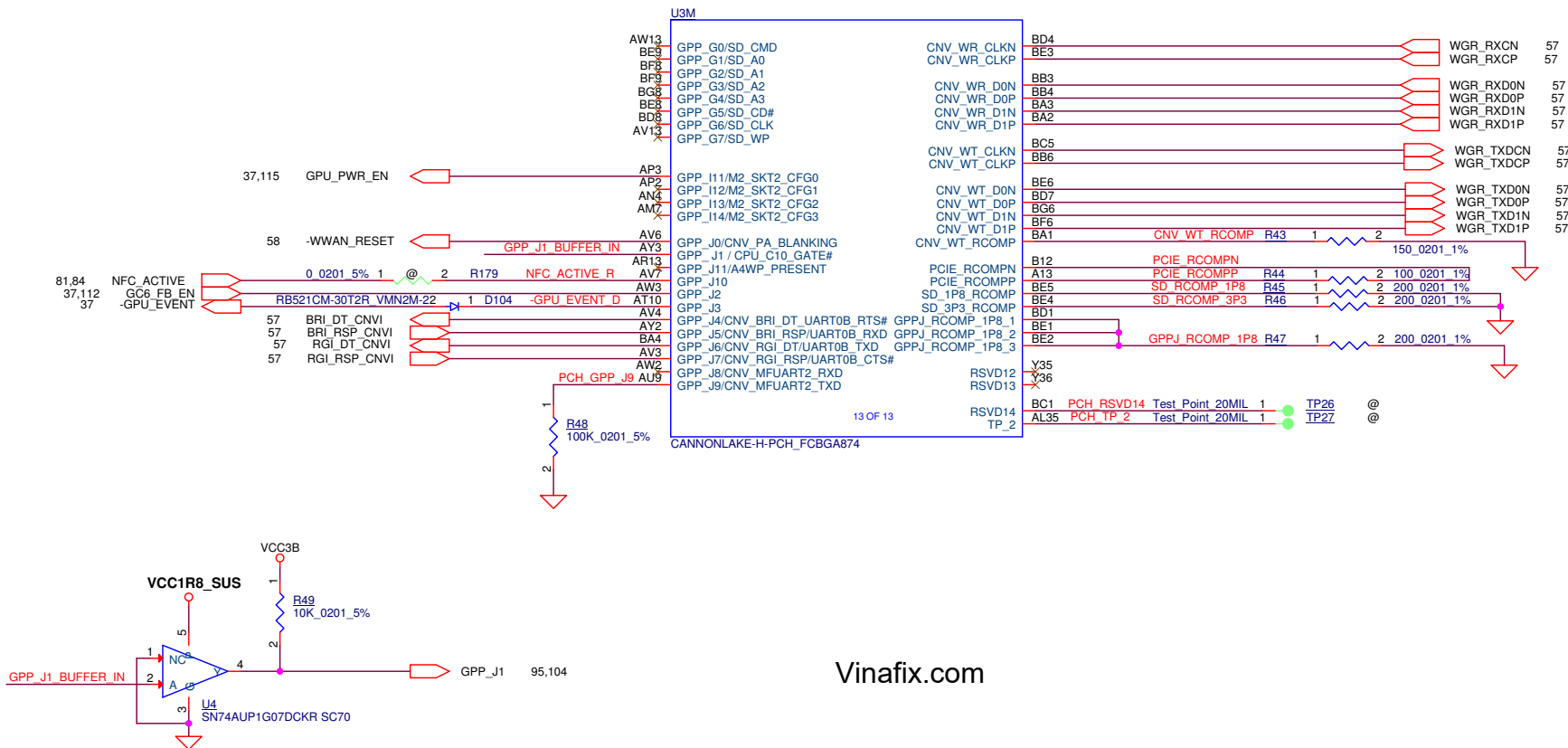
CPU



CPU



PCH



PCH

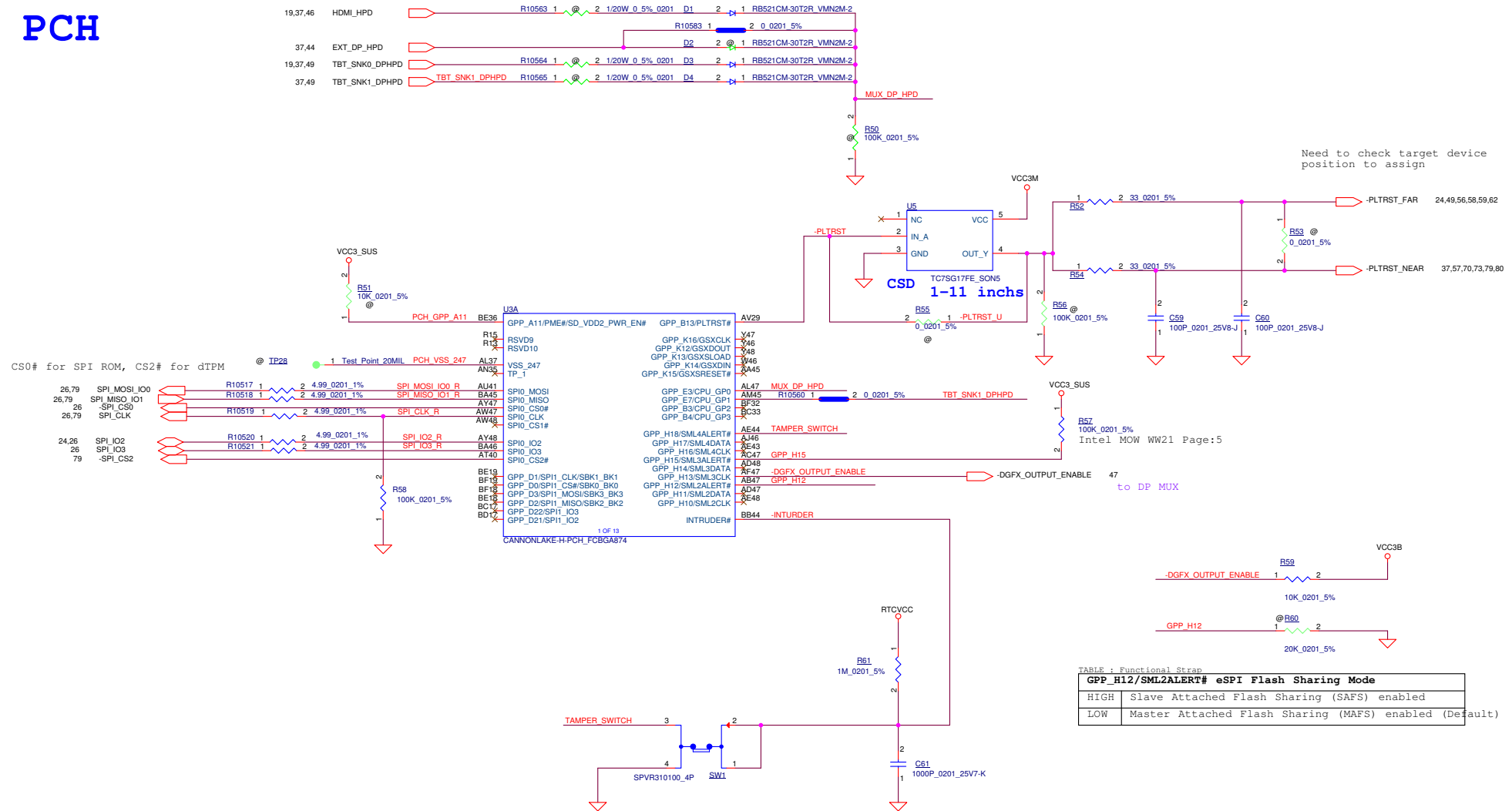


TABLE : Functional Strap	
GPP_H12/SML2ALERT# eSPI Flash Sharing Mode	
HIGH	Slave Attached Flash Sharing (SAFS) enabled
LOW	Master Attached Flash Sharing (MAFS) enabled (Default)

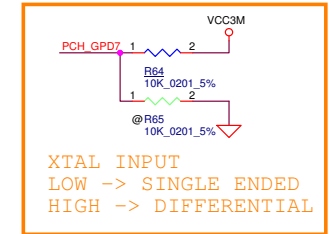
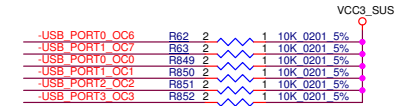
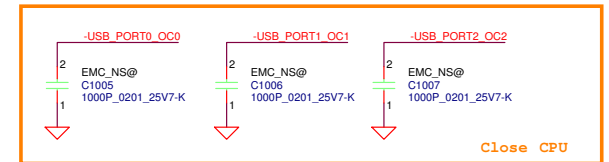
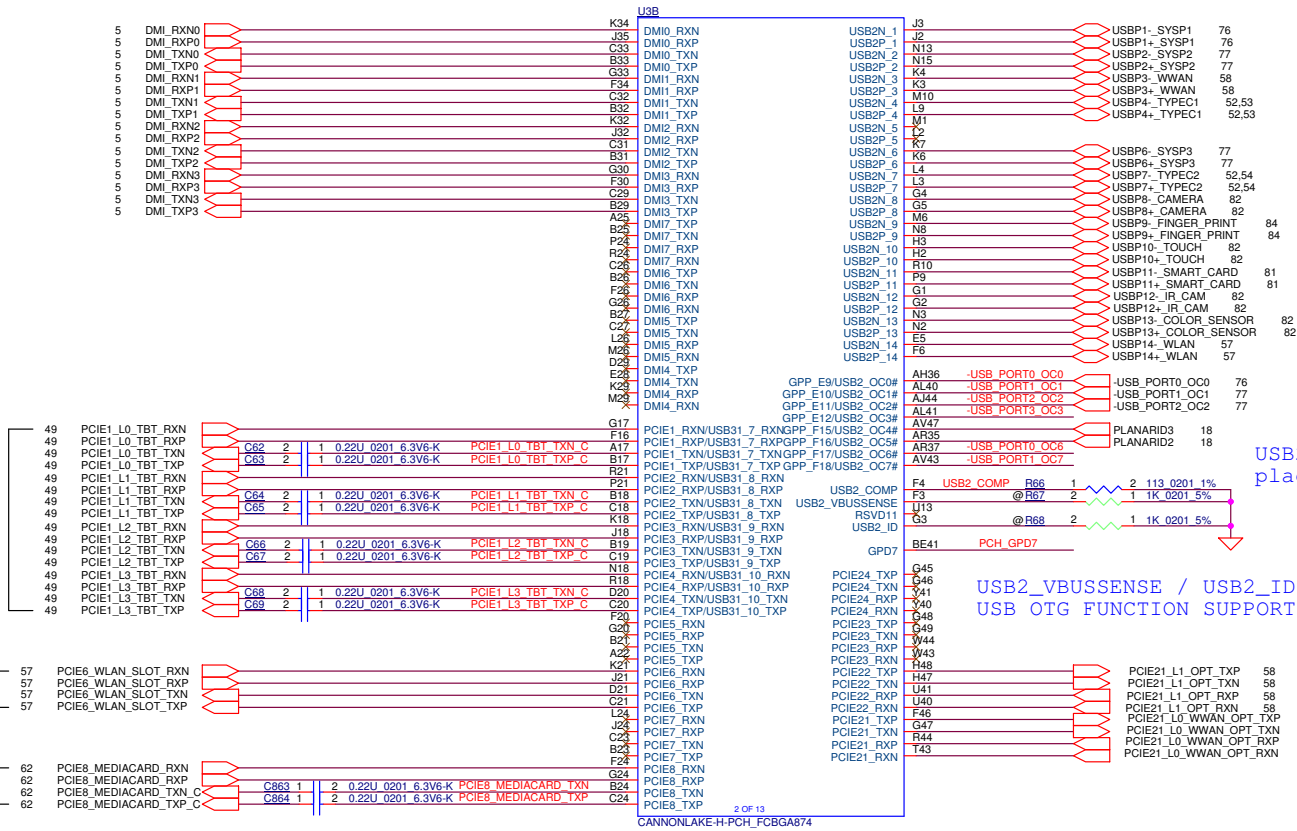
DOOR	SWITCH	-INTRUDER
CLOSE	OPEN	HIGH
OPEN	CLOSE	LOW (ACTIVE

PCH

Thunderbolt
x 4

WLAN Card

Media Card



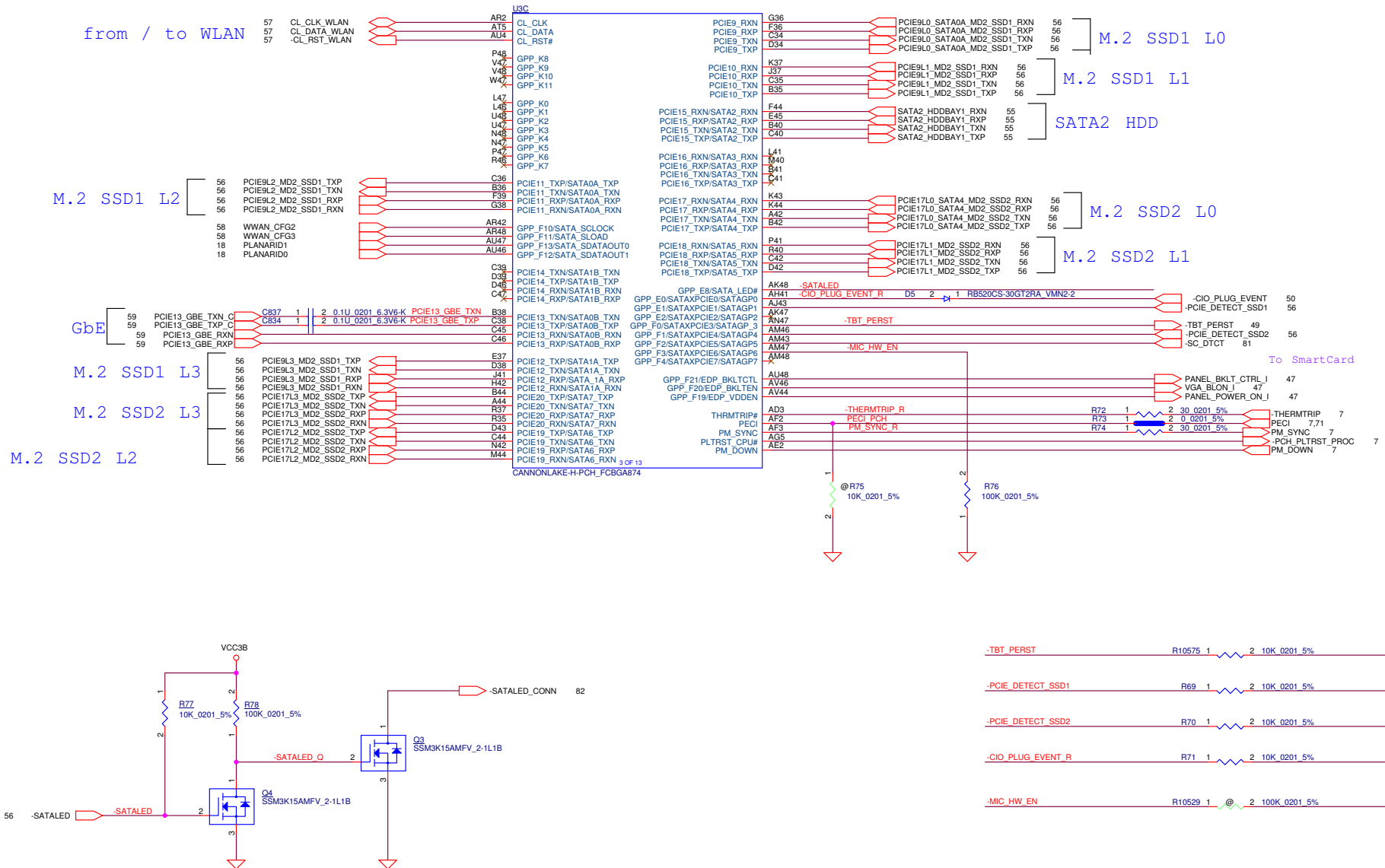
USB2_COMP RES:
place within 1 inch.

USB2_VBUSSENSE / USB2_ID
USB OTG FUNCTION SUPPORT

Optane
x 2

WLAN and OptaneCard

PCH

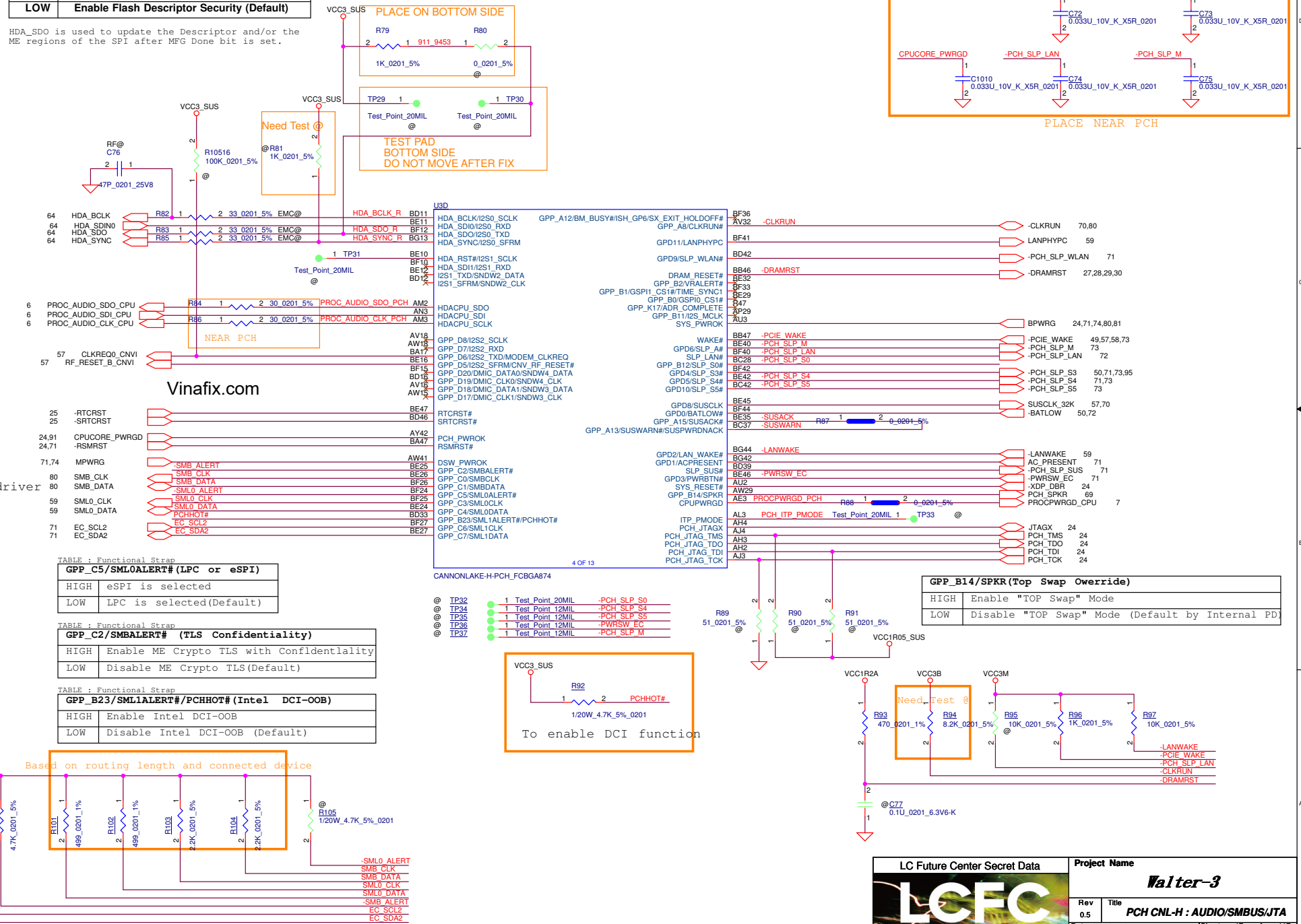


PCH

TABLE : Functional Strap

HDA_SDO/I2S0_TXD	
Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)

HDA_SDO is used to update the Descriptor and/or the ME regions of the SPI after MFG Done bit is set.




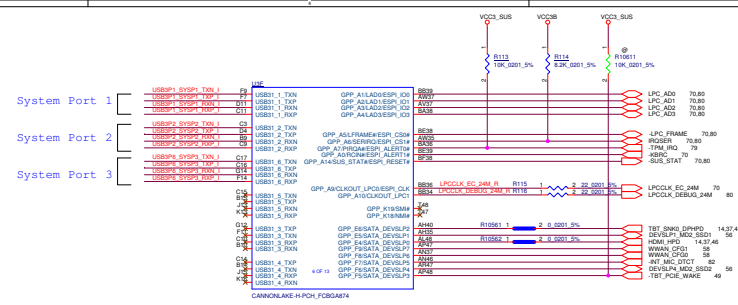
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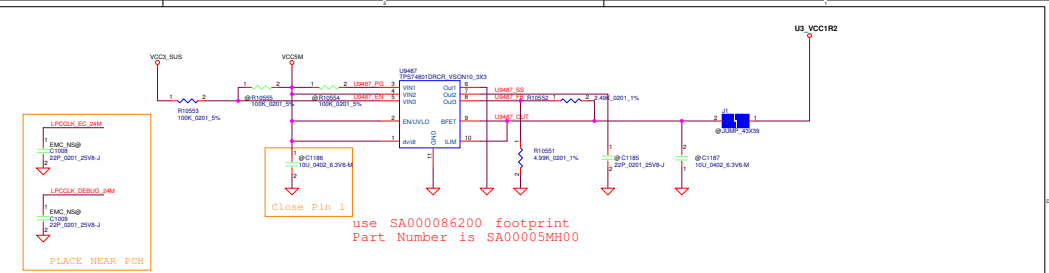
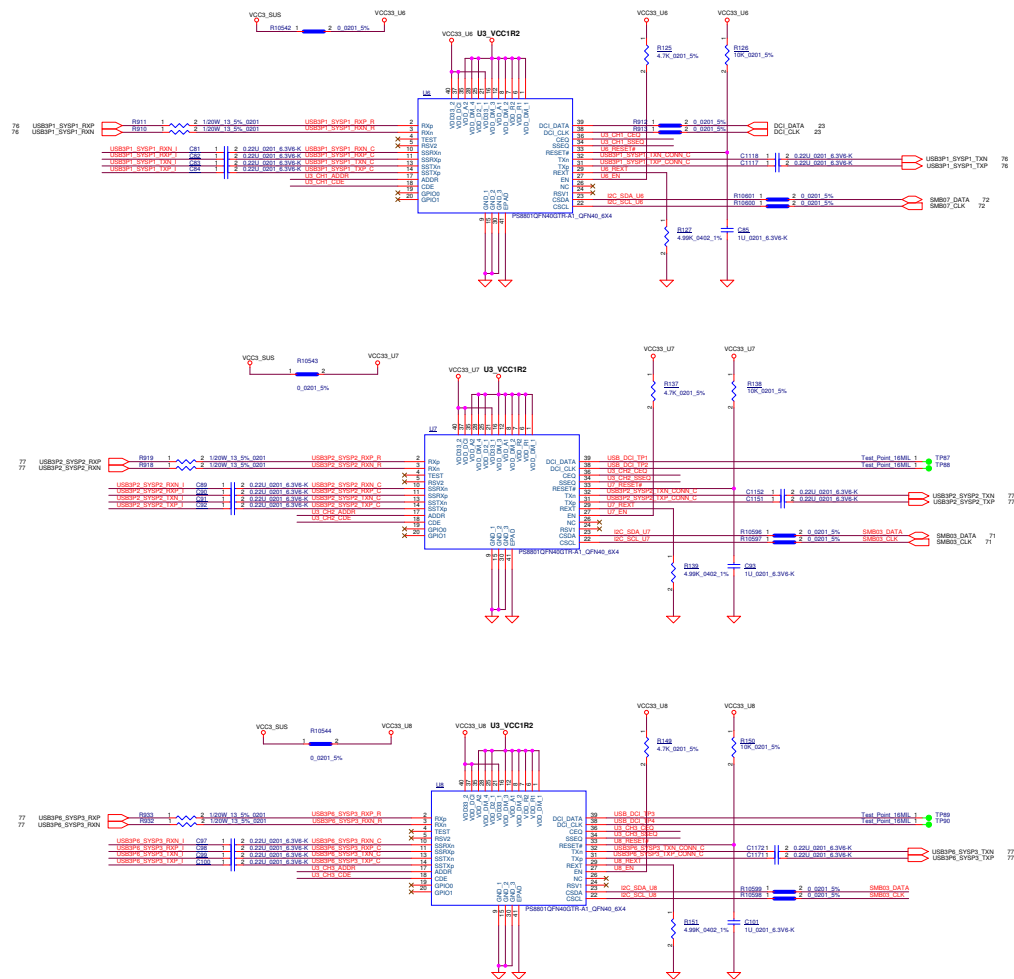
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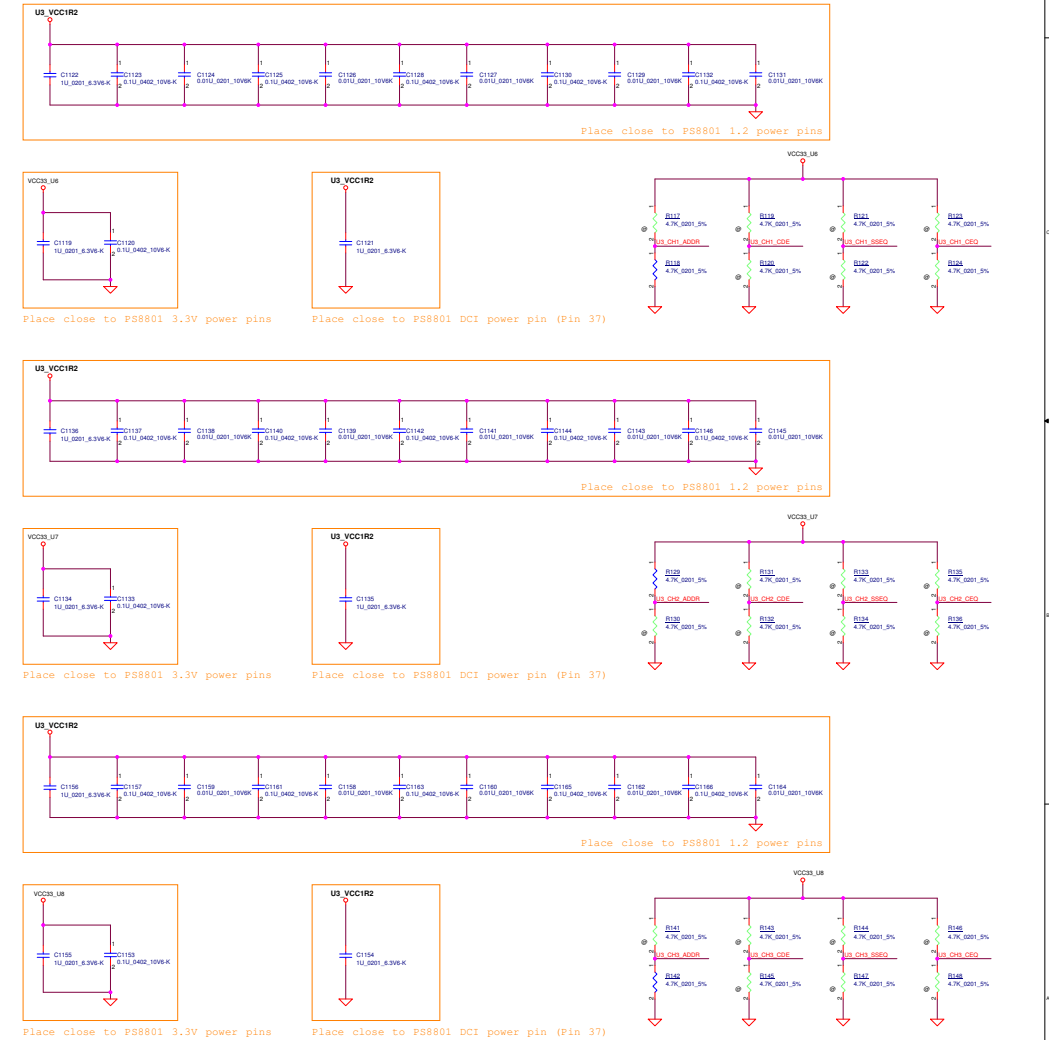
LC Future Center Secret Data		Project Name	
		<i>Walter-3</i>	
		Rev 0.5	Title PCH CNL-H : DDI CONTROL
		Date: Monday, June 25, 2018	Sheet 18 of 117



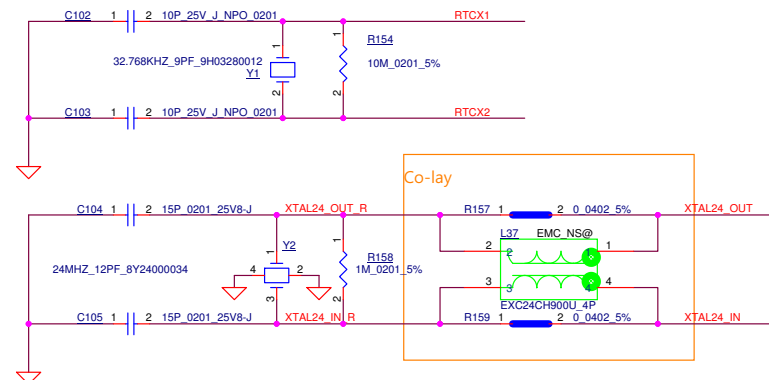
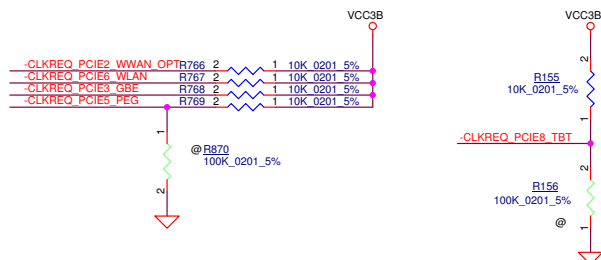
USB3.1 Redriver



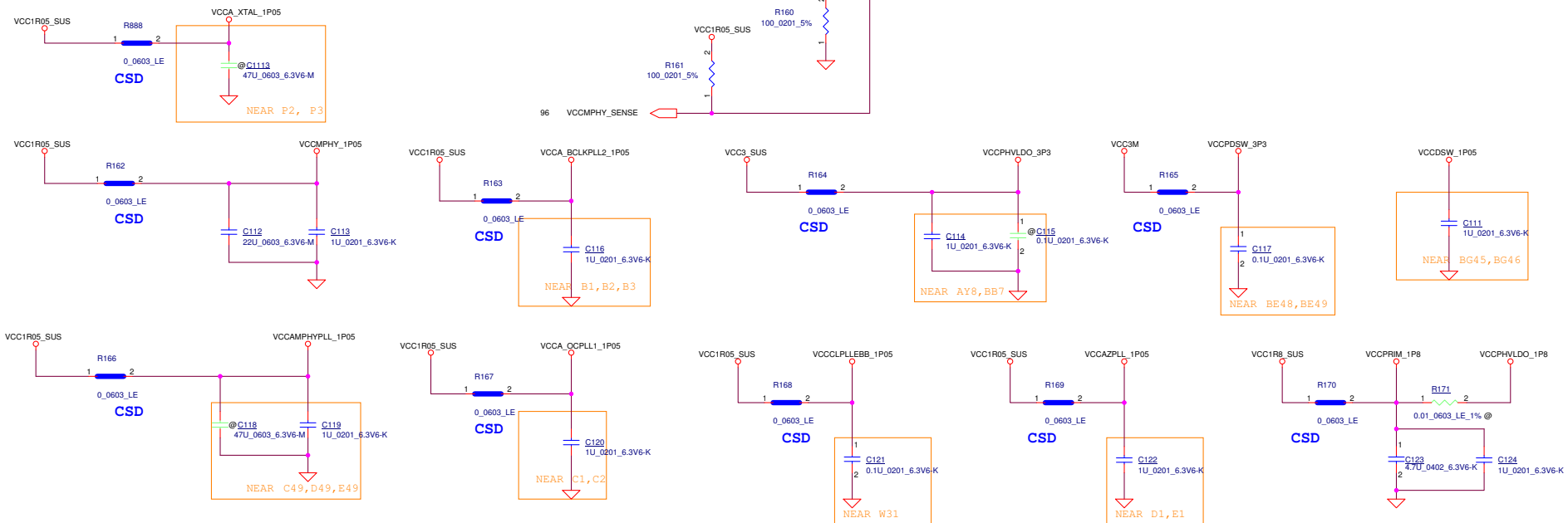
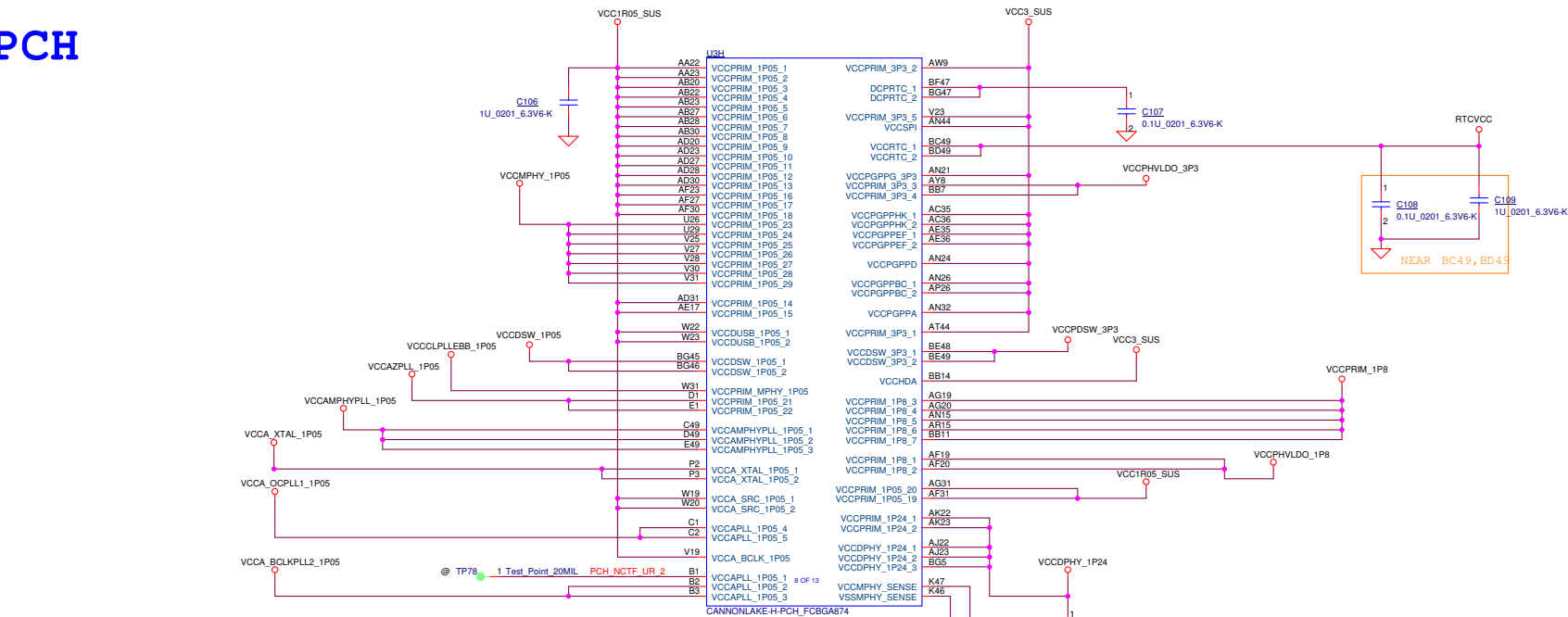
Vinafix.com



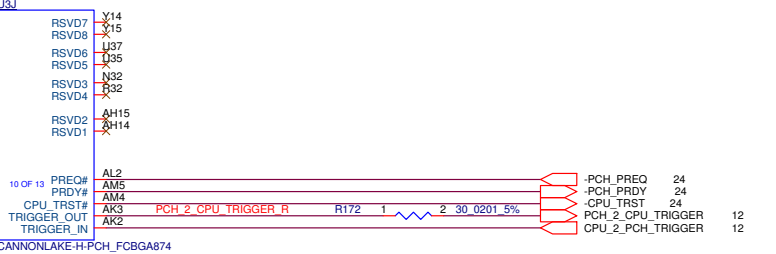
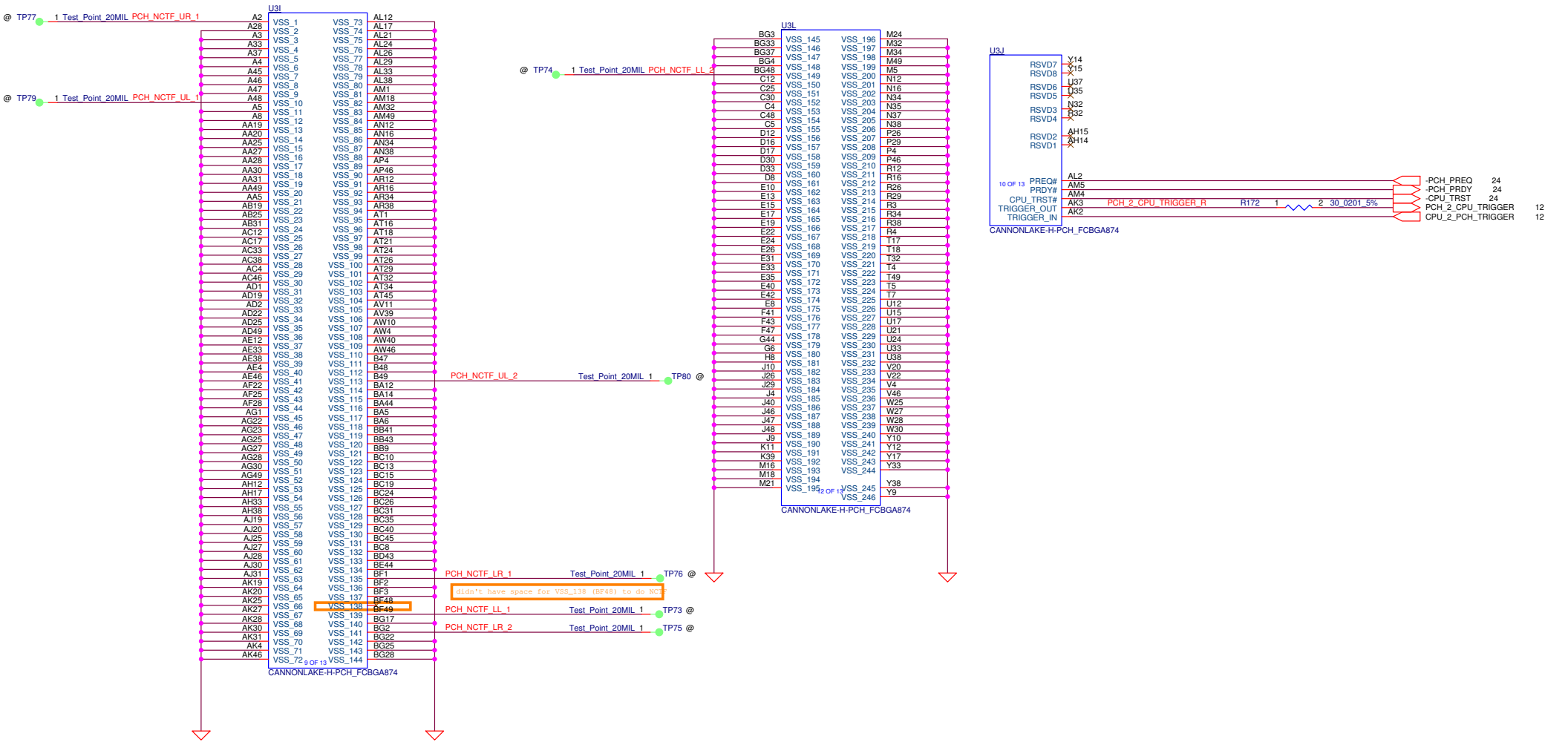
External Pull on CLKREQ# should be placed in device page,
as power railis may be different from PCH-H..



PCH

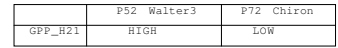


PCH



GPP_B18/GSPI0_MOSI (No Reboot)		PCHR96
HIGH	Enable "No Reboot" Mode	ASM
LOW	Disable "No Reboot" Mode (Default)	NO ASM

← LOGIC



XDP

TABLE : CPU ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
XDPR1	NO ASM	NO ASM	ASM
XDPR2	NO ASM	NO ASM	ASM
XDPR3	NO ASM	NO ASM	ASM
XDPR4	NO ASM	NO ASM	ASM
XDPR5	NO ASM	NO ASM	ASM
XDPR6	NO ASM	NO ASM	ASM
XDPR7	NO ASM	NO ASM	ASM
XDPR27	NO ASM	ASM	NO ASM
XDPR28	NO ASM	ASM	NO ASM
XDPR11	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
XDPC1	NO ASM	ASM	NO ASM
PCHR142	ASM	ASM	ASM
XDPR23	NO ASM	ASM	NO ASM
XDPR14	NO ASM	ASM	ASM
XDPR16	NO ASM	ASM	ASM
XDPR19	NO ASM	ASM	ASM
XDPR20	NO ASM	ASM	ASM
XDPR17	NO ASM	ASM	ASM
XDPR18	NO ASM	ASM	ASM
XDPR22	NO ASM	ASM	ASM
XDPR24	NO ASM	ASM	ASM
XDPR25	NO ASM	ASM	ASM
XDPR26	NO ASM	ASM	ASM

LOGIC

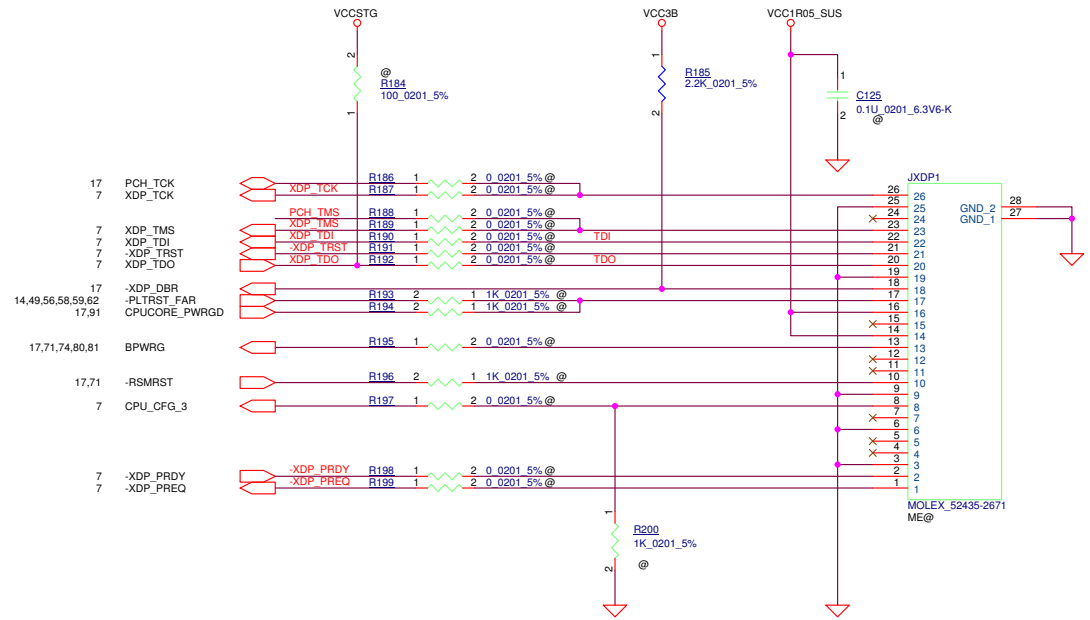
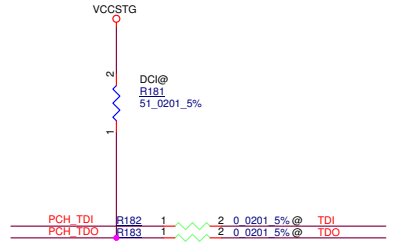
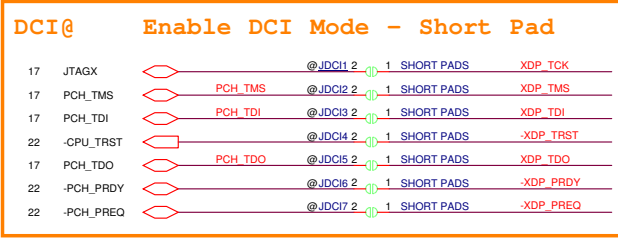
TABLE : PCH ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
XDPR8	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
XDPR21	NO ASM	ASM	NO ASM
XDPR23	NO ASM	ASM	NO ASM
XDPR13	NO ASM	ASM	NO ASM
XDPR15	NO ASM	ASM	NO ASM
XDPR9	NO ASM	ASM	NO ASM
XDPR10	NO ASM	ASM	NO ASM

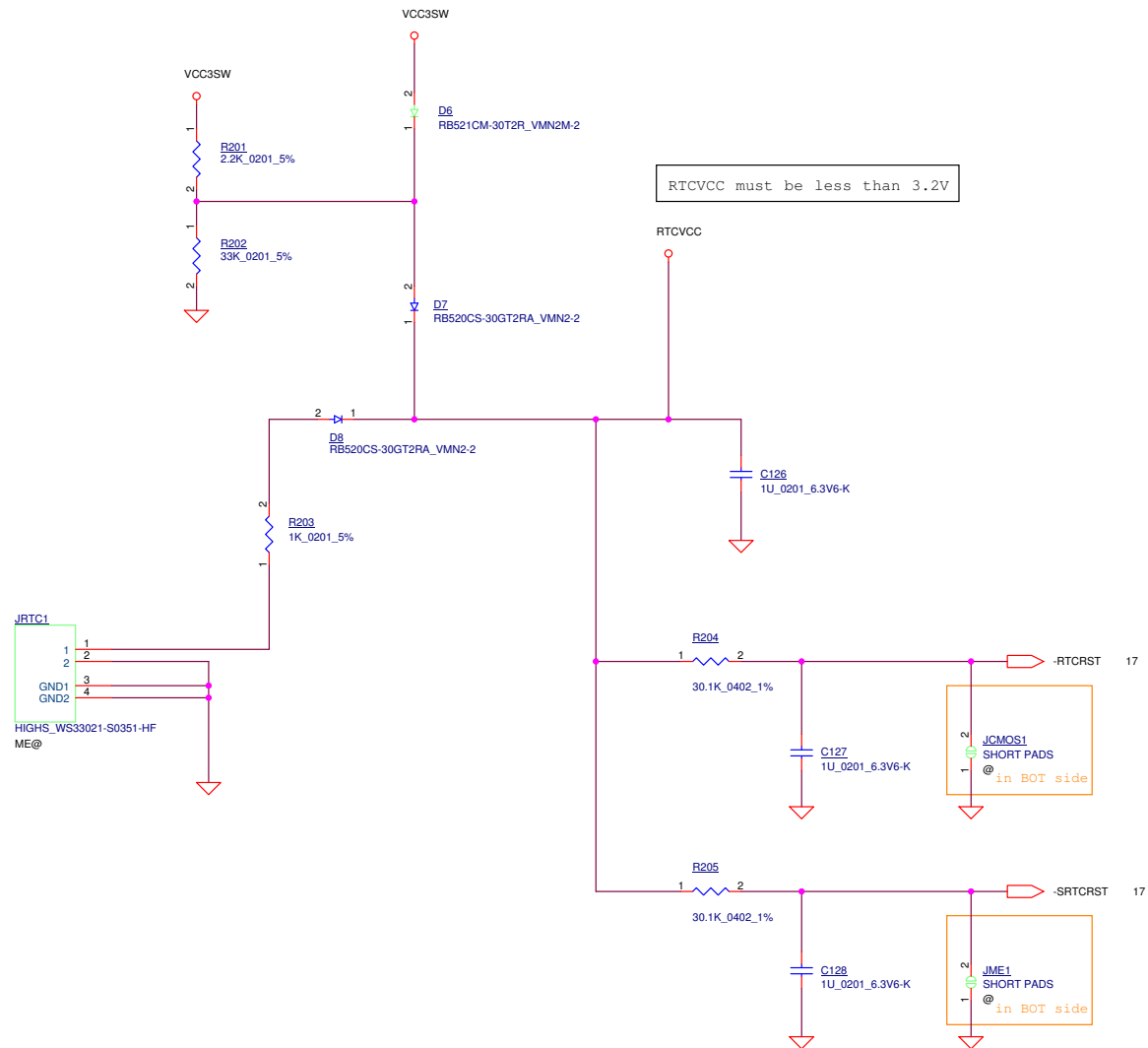
LOGIC

PCHR31	NO ASM	ASM	NO ASM
PCHR32	NO ASM	ASM	NO ASM
PCHR33	NO ASM	ASM	NO ASM

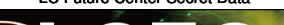
SHEET 17



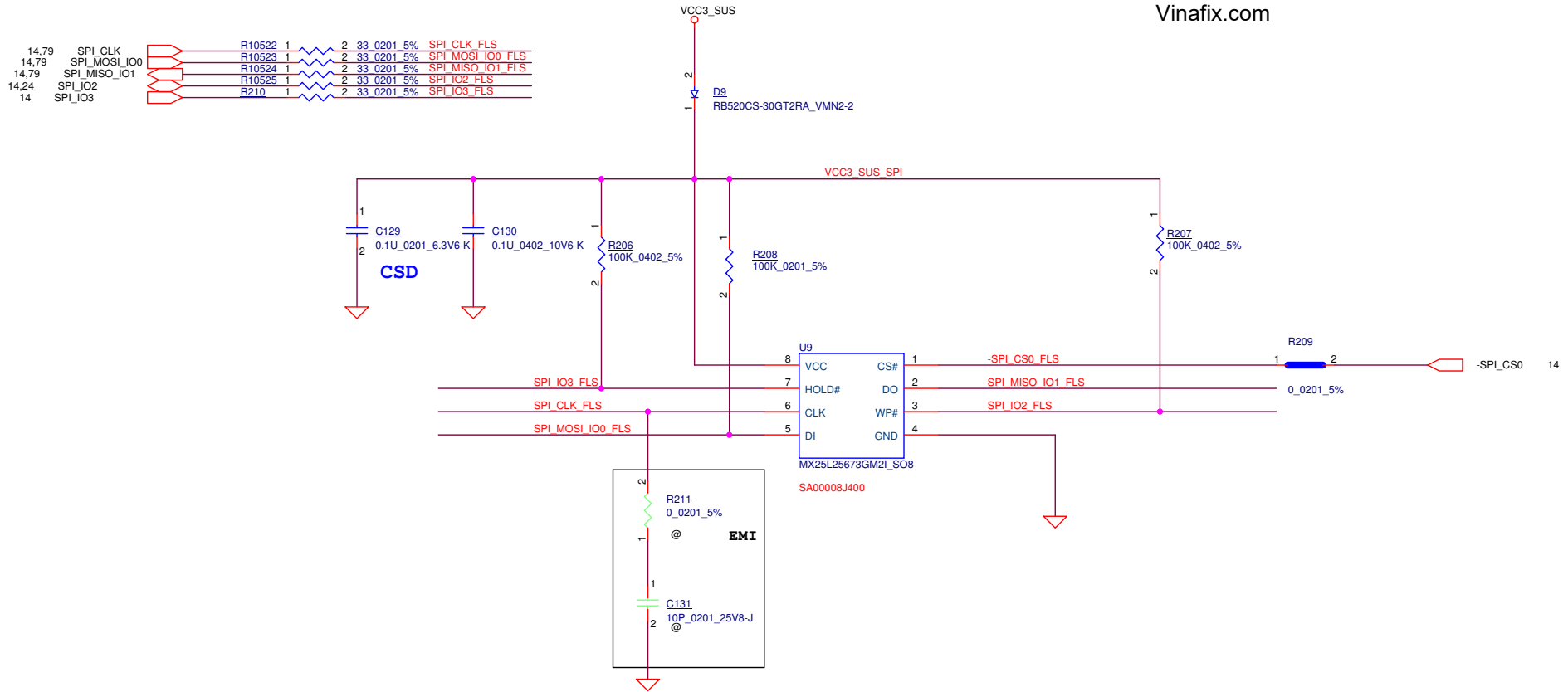
RTC




RTCVCC must be less than 3.2V

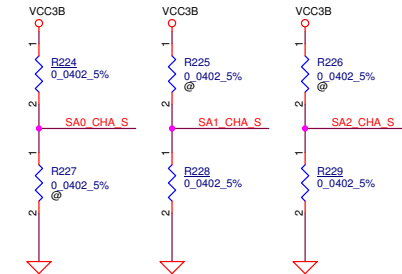
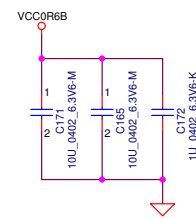
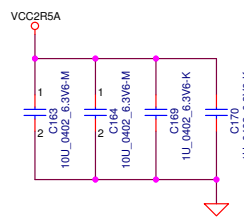
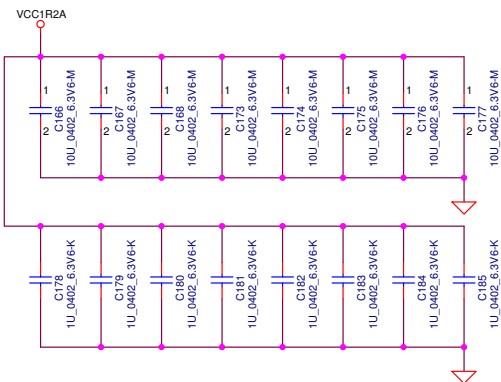
LC Future Center Secret Data		Project Name	
		<i>Walter-3</i>	
		Rev 0.5	Title RTC BATTERY
		Date: Monday, June 25, 2018	
		Sheet	25 of 117

SPI FLASH

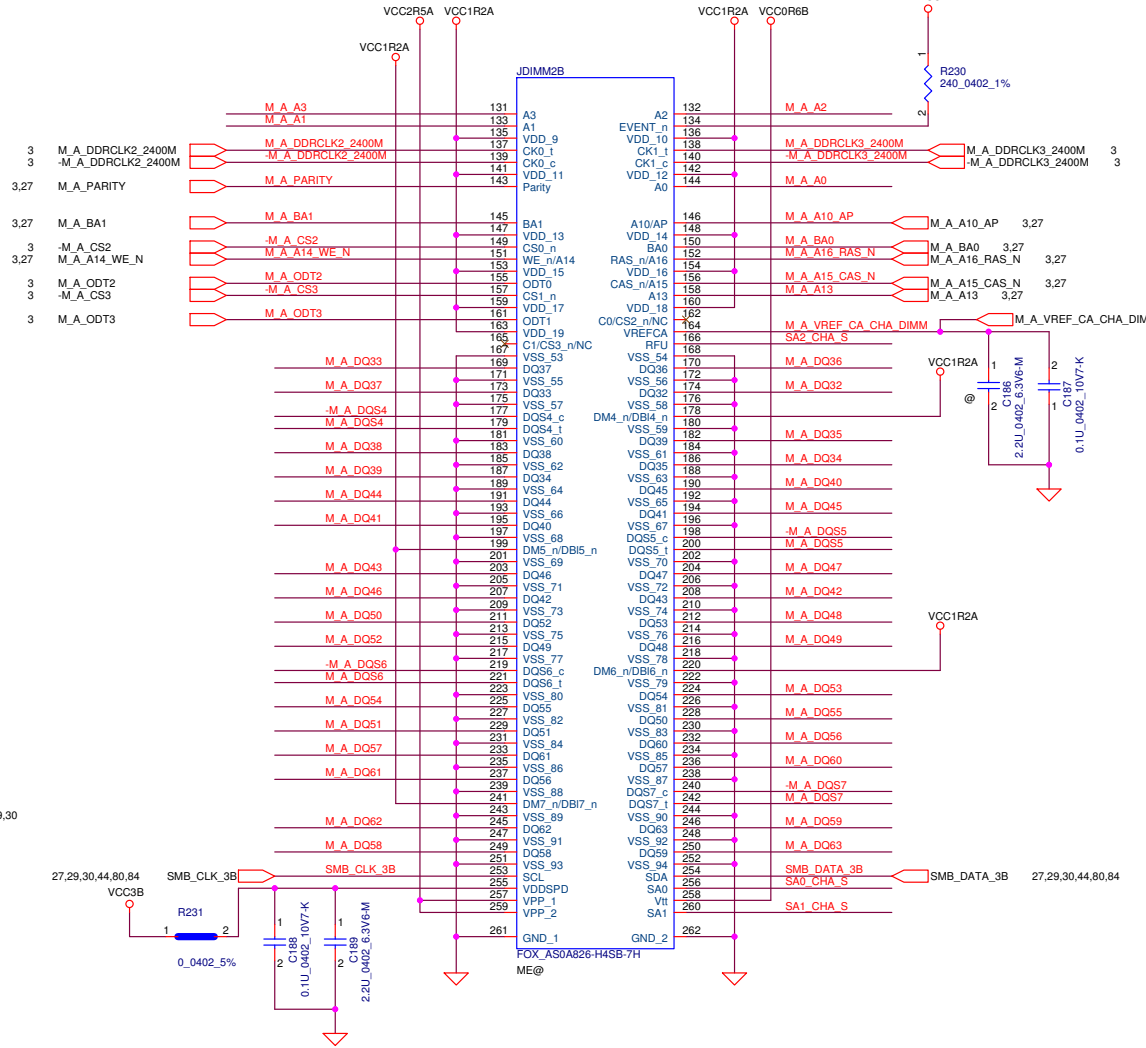
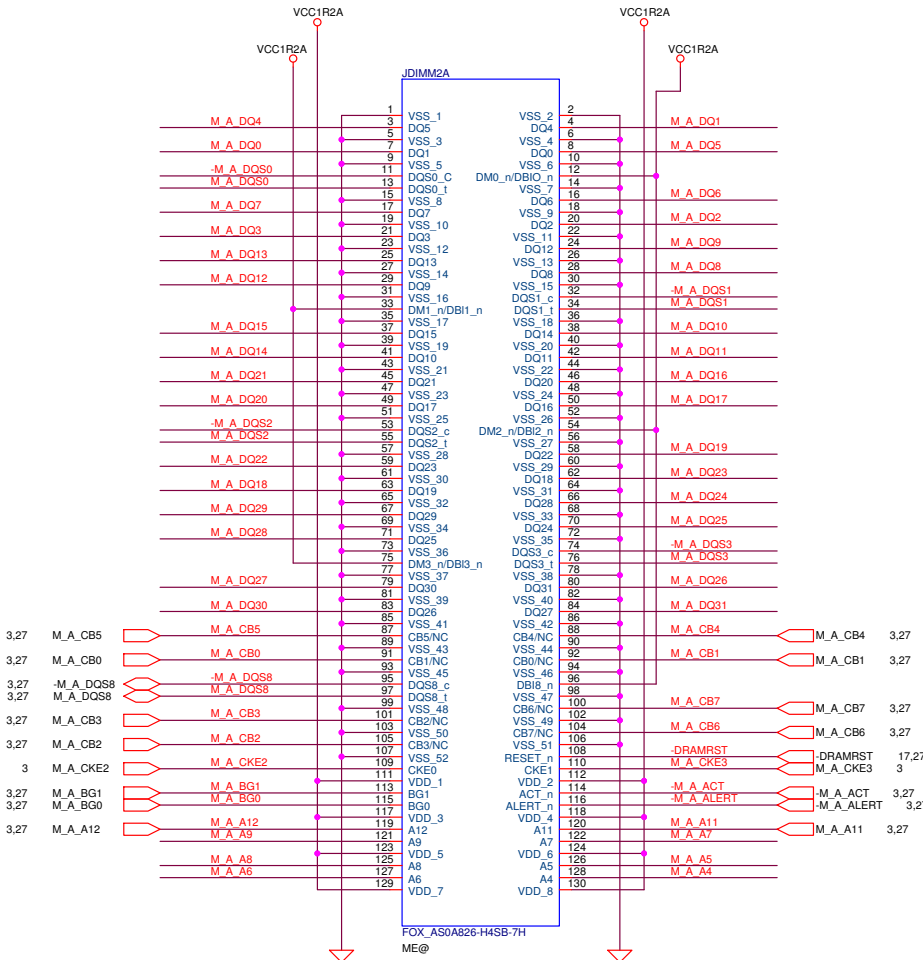


LC Future Center Secret Data		Project Name	
		Walter-3	
Rev	Title		
0.5	SPI FLASH		
Date: Monday, June 25, 2018		Sheet	26 of 117

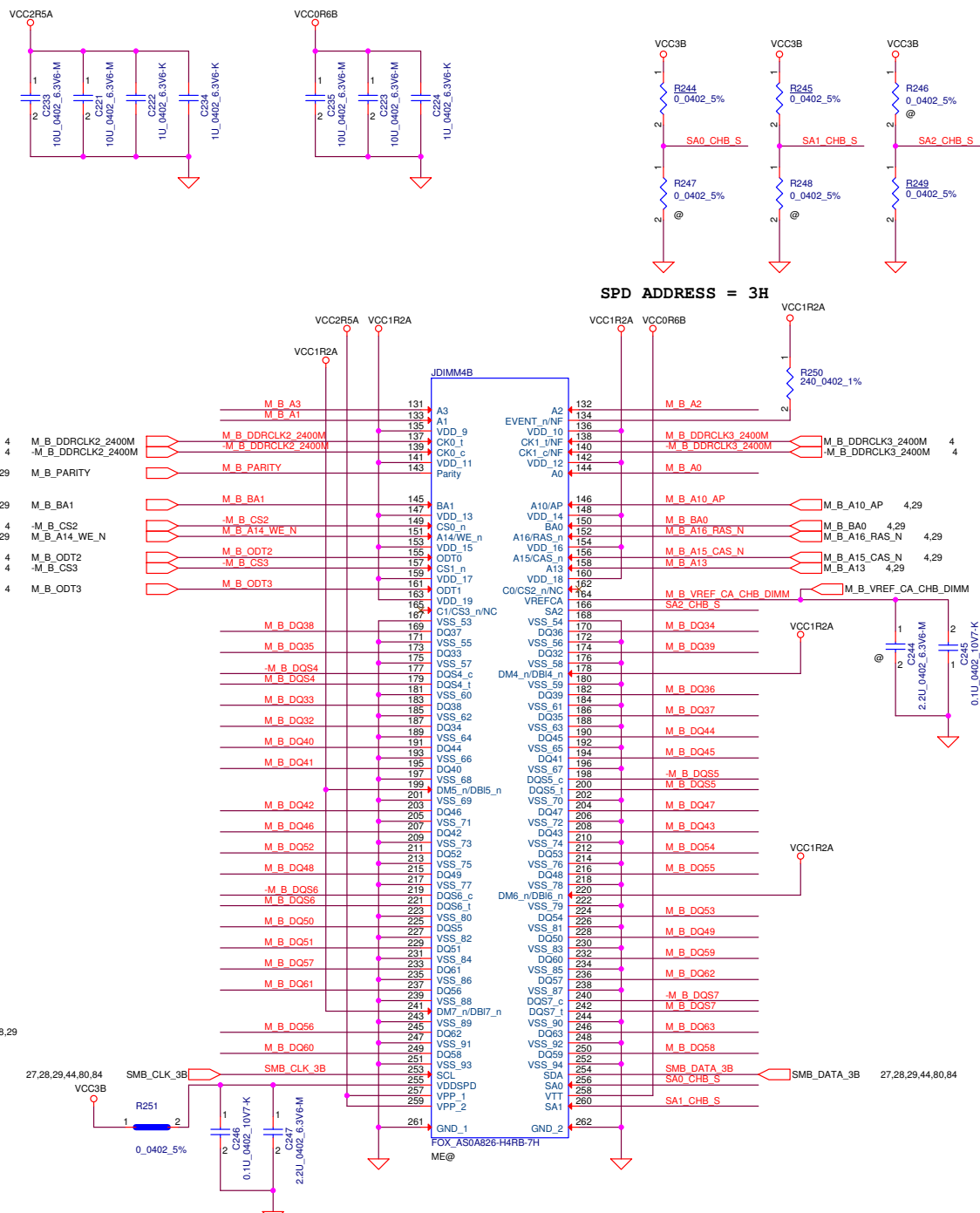
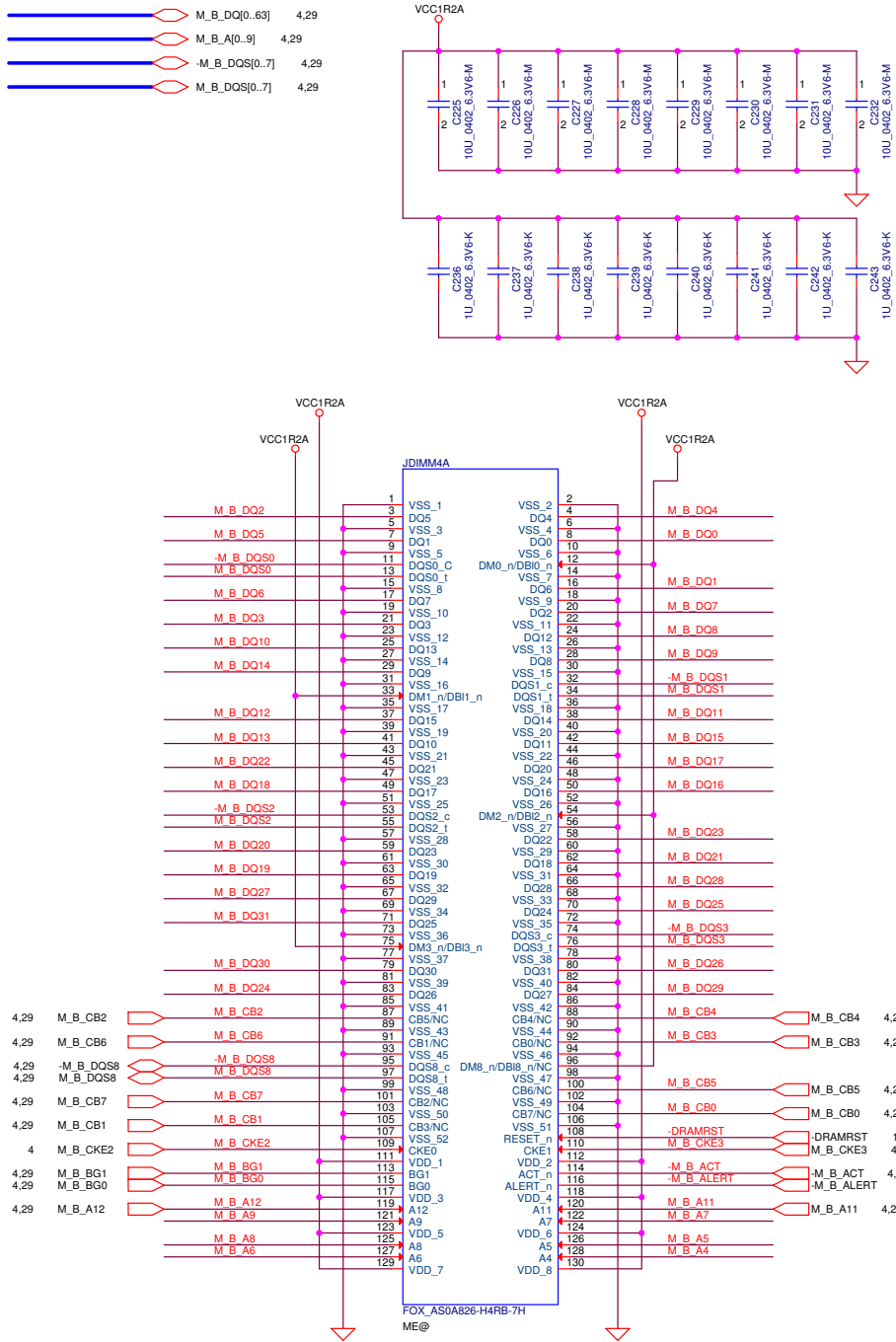
M_A_DQ[0..63] 3,27
M_A_A[0..9] 3,27
-M_A_DQS[0..7] 3,27
M_A_DQS[0..7] 3,27



SPD ADDRESS = 1H

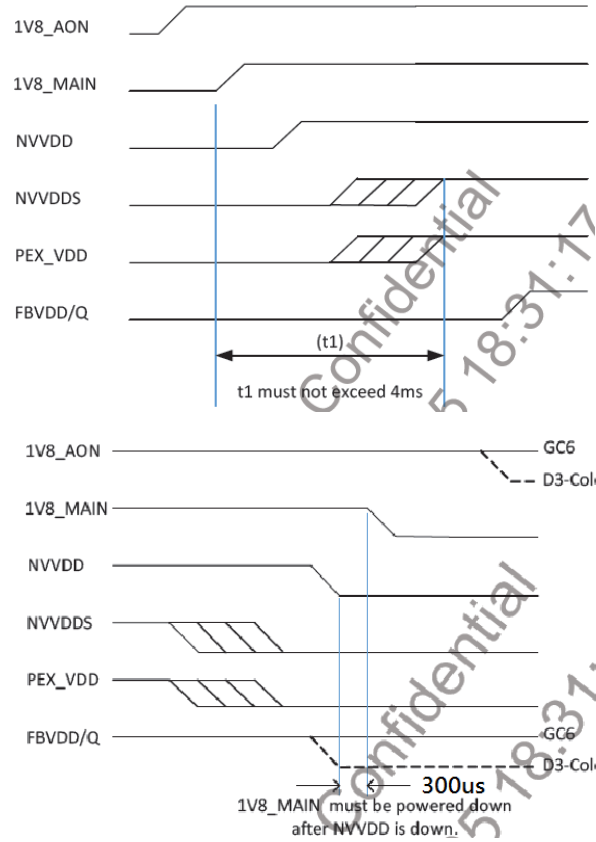
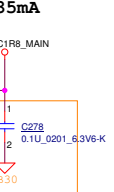
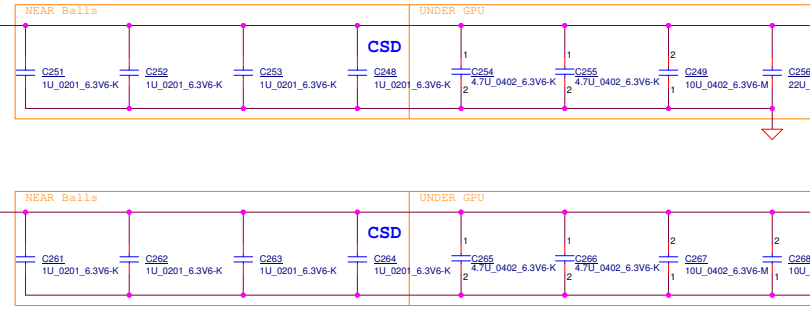


Payton Common



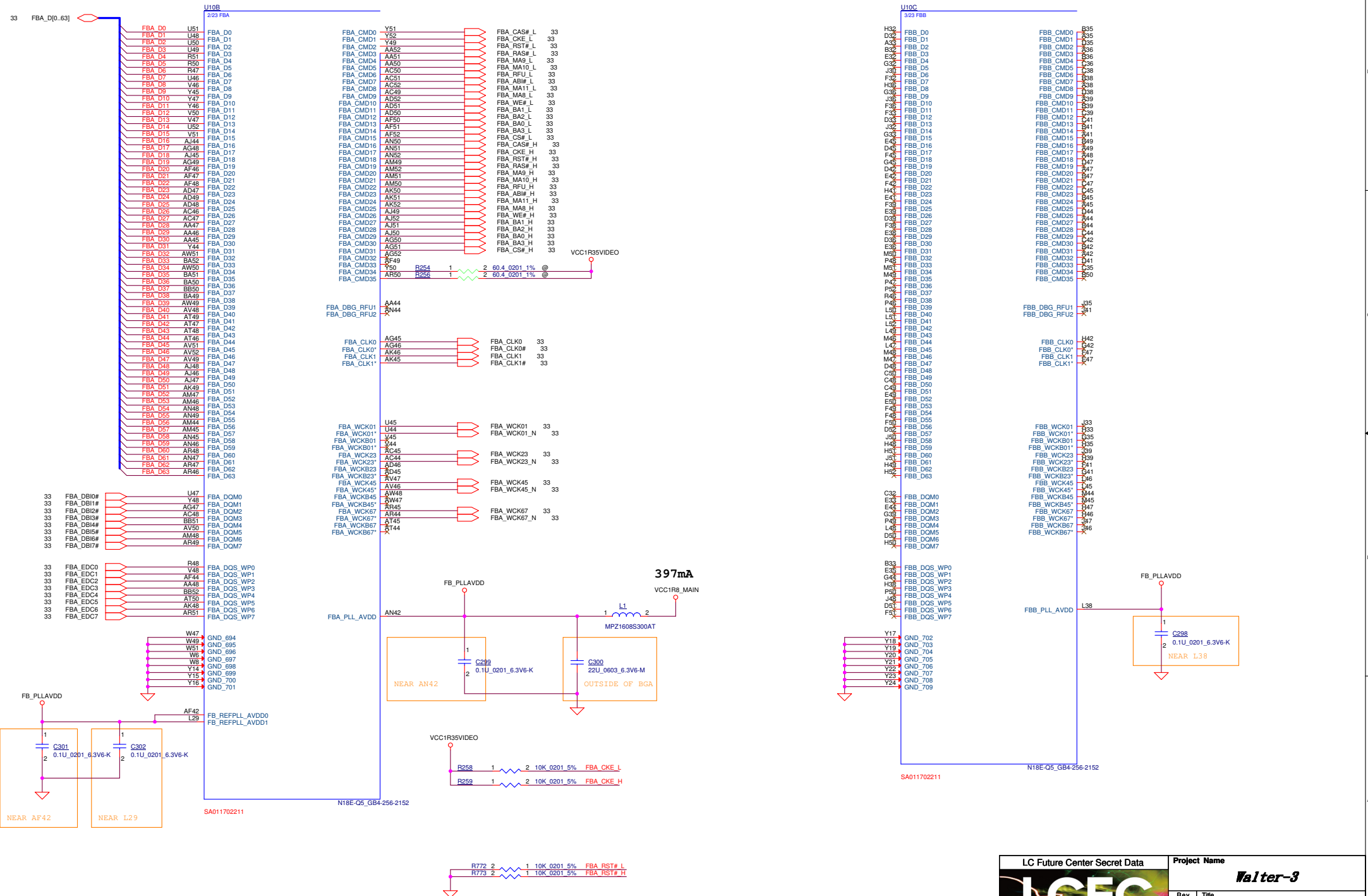
Payton Common

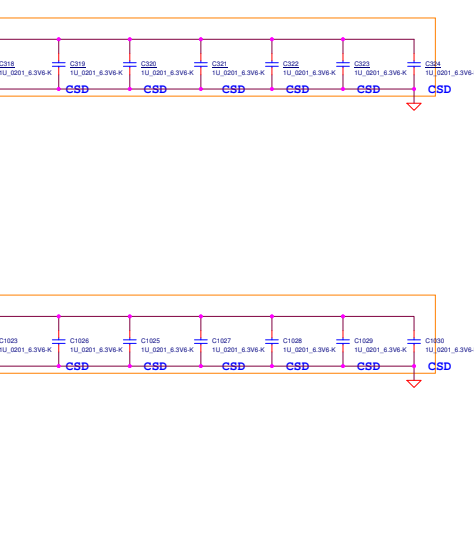
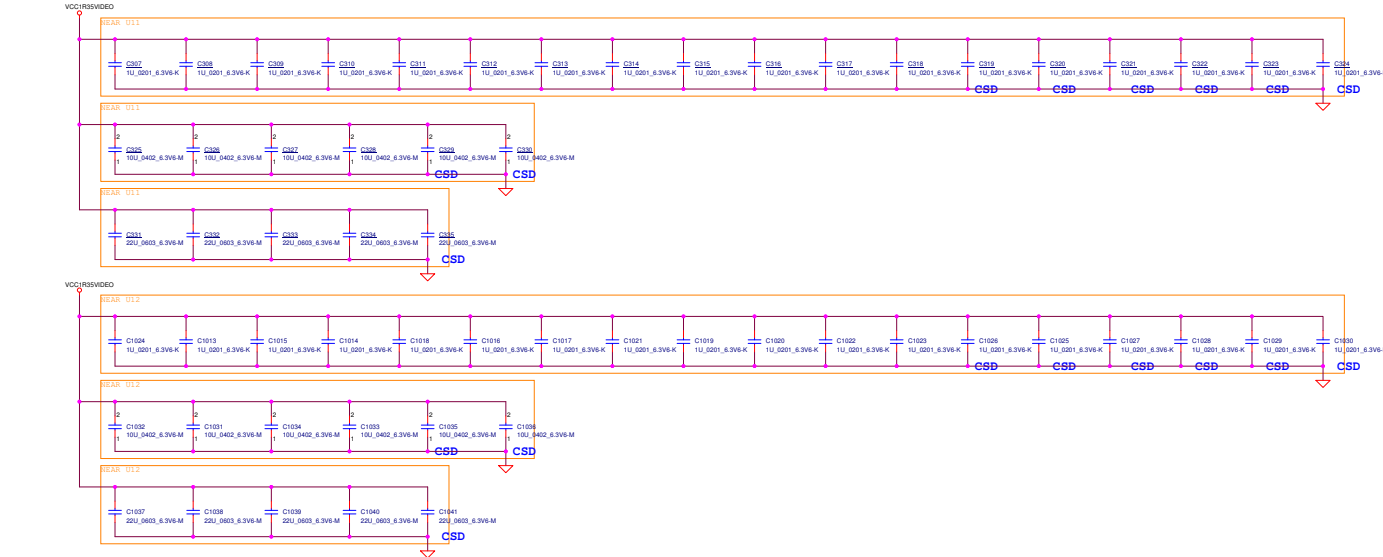
GPU

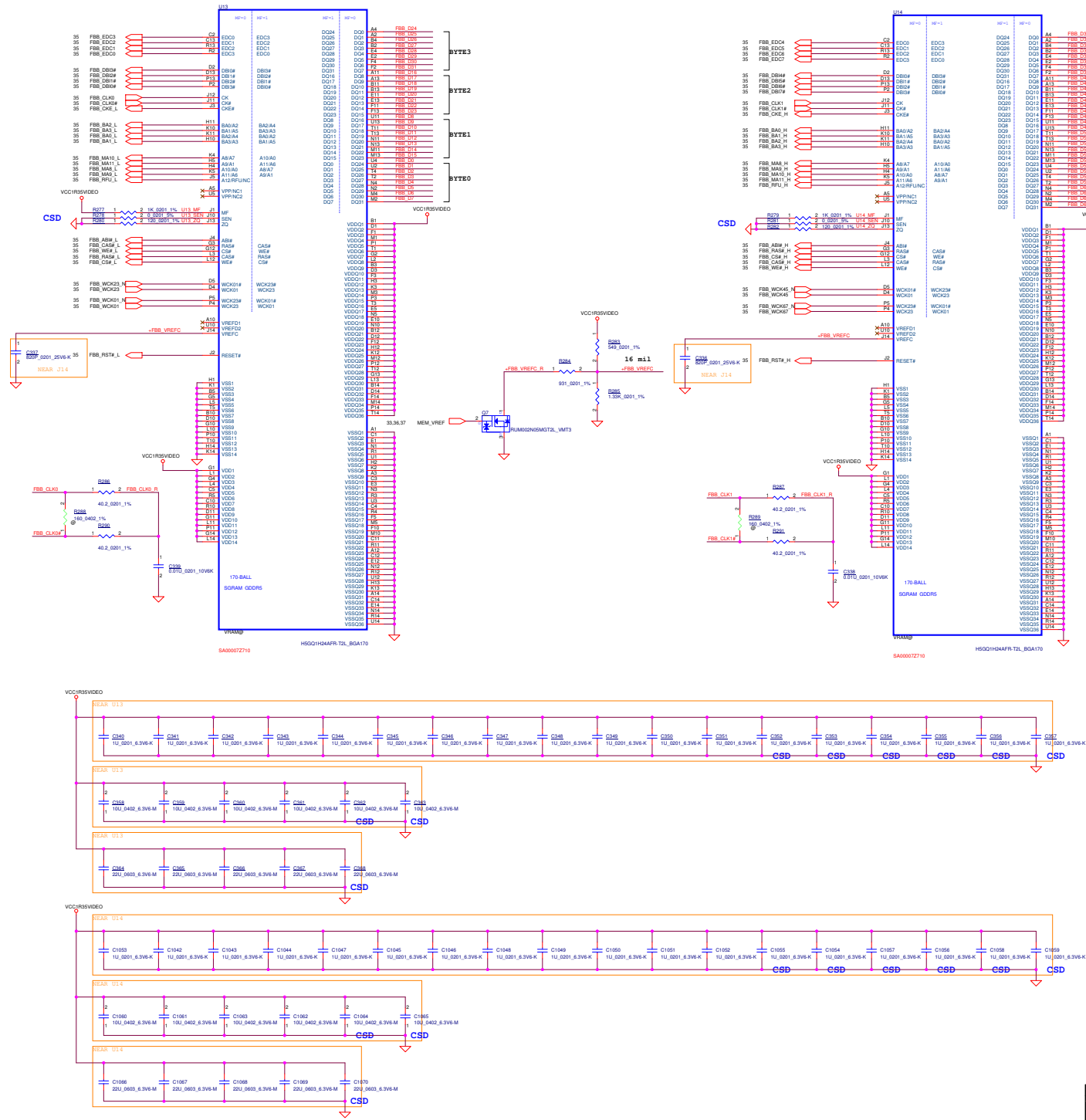


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GPU







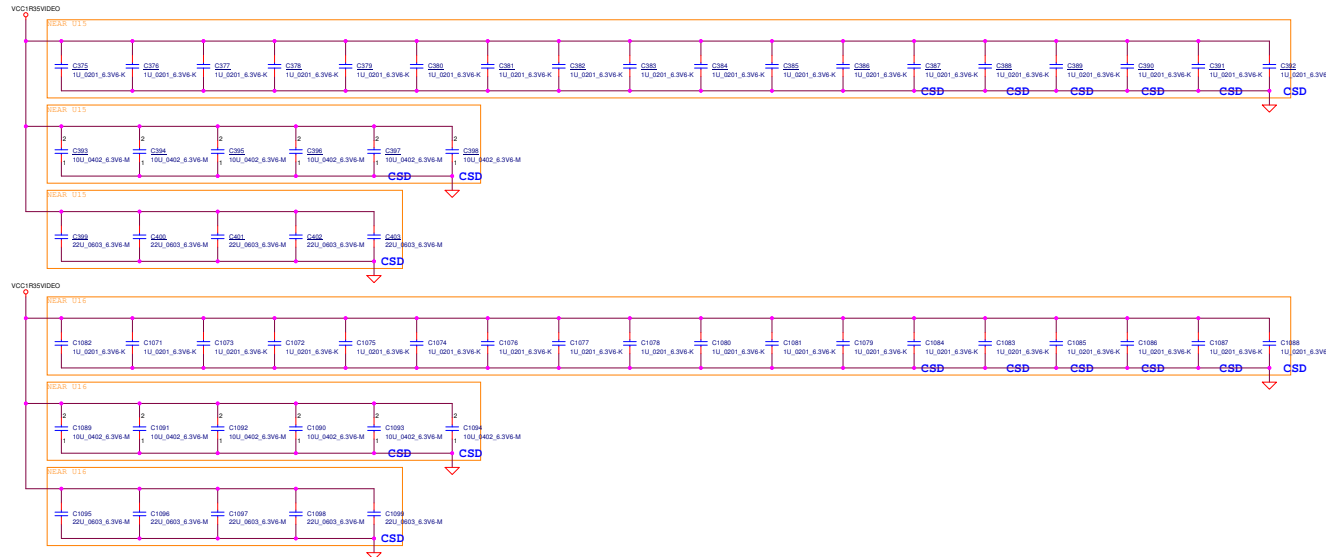
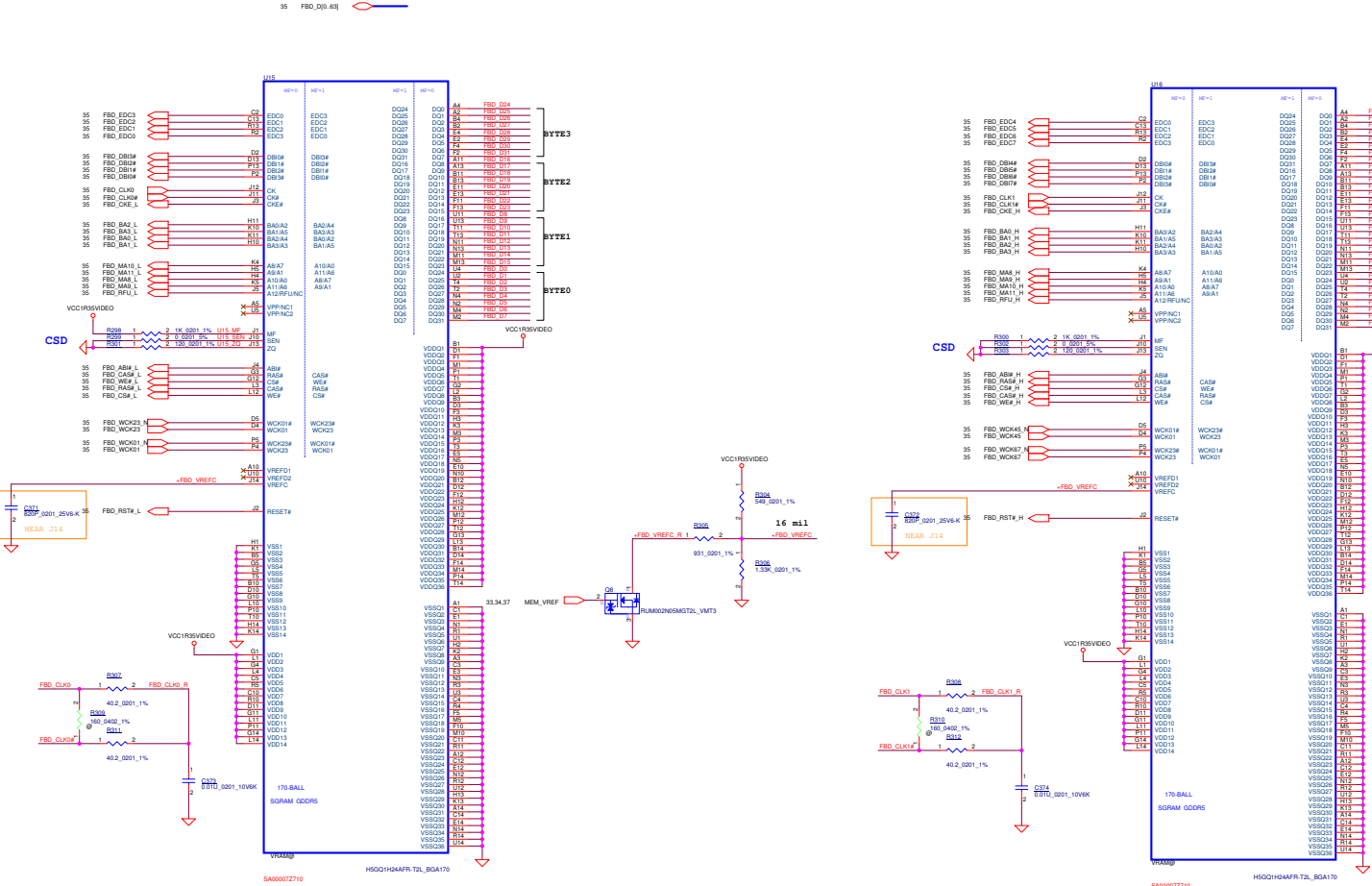
The image displays two detailed PCB layout diagrams for the FBB and FBD components of the SA011702211 board. The left diagram shows the FBB component with its various pins connected to the board's internal components and power planes. The right diagram shows the FBD component with similar connections. Both diagrams include a detailed pinout table for each component, showing the connection of various pins to the board's internal components and power planes. The diagrams are color-coded to show different types of connections and components.

FBB Component Pinout:

FBB Pin	Board Pin	Board Component
FBB_D0	C6	FBC_D0
FBB_D1	D6	FBC_D1
FBB_D2	A6	FBC_D2
FBB_D3	B6	FBC_D3
FBB_D4	B4	FBC_D4
FBB_D5	A4	FBC_D5
FBB_D6	B3	FBC_D6
FBB_D7	C4	FBC_D7
FBB_D8	D9	FBC_D8
FBB_D9	C9	FBC_D9
FBB_D10	E9	FBC_D10
FBB_D11	B9	FBC_D11
FBB_D12	B8	FBC_D12
FBB_D13	A8	FBC_D13
FBB_D14	F6	FBC_D14
FBB_D15	E6	FBC_D15
FBB_D16	F18	FBC_D16
FBB_D17	G18	FBC_D17
FBB_D18	E18	FBC_D18
FBB_D19	H18	FBC_D19
FBB_D20	D15	FBC_D20
FBB_D21	E15	FBC_D21
FBB_D22	G17	FBC_D22
FBB_D23	H17	FBC_D23
FBB_D24	J15	FBC_D24
FBB_D25	H15	FBC_D25
FBB_D26	E14	FBC_D26
FBB_D27	F14	FBC_D27
FBB_D28	H11	FBC_D28
FBB_D29	G11	FBC_D29
FBB_D30	F11	FBC_D30
FBB_D31	E11	FBC_D31
FBB_D32	J9	FBC_D32
FBB_D33	F9	FBC_D33
FBB_D34	H29	FBC_D34
FBB_D35	G30	FBC_D35
FBB_D36	E30	FBC_D36
FBB_D37	A30	FBC_D37
FBB_D38	H30	FBC_D38
FBB_D39	C30	FBC_D39
FBB_D40	D27	FBC_D40
FBB_D41	J26	FBC_D41
FBB_D42	F27	FBC_D42
FBB_D43	G27	FBC_D43
FBB_D44	C27	FBC_D44
FBB_D45	B27	FBC_D45
FBB_D46	A27	FBC_D46
FBB_D47	C29	FBC_D47
FBB_D48	H20	FBC_D48
FBB_D49	D18	FBC_D49
FBB_D50	C20	FBC_D50
FBB_D51	E20	FBC_D51
FBB_D52	F23	FBC_D52
FBB_D53	E21	FBC_D53
FBB_D54	D21	FBC_D54
FBB_D55	E23	FBC_D55
FBB_D56	G24	FBC_D56
FBB_D57	H26	FBC_D57
FBB_D58	F24	FBC_D58
FBB_D59	G26	FBC_D59
FBB_D60	F26	FBC_D60
FBB_D61	D26	FBC_D61
FBB_D62	B26	FBC_D62
FBB_D63	C26	FBC_D63

FBD Component Pinout:

FBD Pin	Board Pin	Board Component
FBD_D0	A8	FBD_D0
FBD_D1	A4	FBD_D1
FBD_D2	A2	FBD_D2
FBD_D3	A3	FBD_D3
FBD_D4	A5	FBD_D4
FBD_D5	A6	FBD_D5
FBD_D6	A9	FBD_D6
FBD_D7	A7	FBD_D7
FBD_D8	A4	FBD_D8
FBD_D9	A9	FBD_D9
FBD_D10	A6	FBD_D10
FBD_D11	A5	FBD_D11
FBD_D12	A4	FBD_D12
FBD_D13	A5	FBD_D13
FBD_D14	A6	FBD_D14
FBD_D15	A6	FBD_D15
FBD_D16	A6	FBD_D16
FBD_D17	A6	FBD_D17
FBD_D18	A6	FBD_D18
FBD_D19	A6	FBD_D19
FBD_D20	A6	FBD_D20
FBD_D21	A6	FBD_D21
FBD_D22	A6	FBD_D22
FBD_D23	A6	FBD_D23
FBD_D24	A6	FBD_D24
FBD_D25	A6	FBD_D25
FBD_D26	A6	FBD_D26
FBD_D27	A6	FBD_D27
FBD_D28	A6	FBD_D28
FBD_D29	A6	FBD_D29
FBD_D30	A6	FBD_D30
FBD_D31	A6	FBD_D31
FBD_D32	A6	FBD_D32
FBD_D33	A6	FBD_D33
FBD_D34	A6	FBD_D34
FBD_D35	A6	FBD_D35
FBD_D36	A6	FBD_D36
FBD_D37	A6	FBD_D37
FBD_D38	A6	FBD_D38
FBD_D39	A6	FBD_D39
FBD_D40	A6	FBD_D40
FBD_D41	A6	FBD_D41
FBD_D42	A6	FBD_D42
FBD_D43	A6	FBD_D43
FBD_D44	A6	FBD_D44
FBD_D45	A6	FBD_D45
FBD_D46	A6	FBD_D46
FBD_D47	A6	FBD_D47
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FBD_D52	A6	FBD_D52
FBD_D53	A6	FBD_D53
FBD_D54	A6	FBD_D54
FBD_D55	A6	FBD_D55
FBD_D56	A6	FBD_D56
FBD_D57	A6	FBD_D57
FBD_D58	A6	FBD_D58
FBD_D59	A6	FBD_D59
FBD_D60	A6	FBD_D60
FBD_D61	A6	FBD_D61
FBD_D62	A6	FBD_D62
FBD_D63	A6	FBD_D63

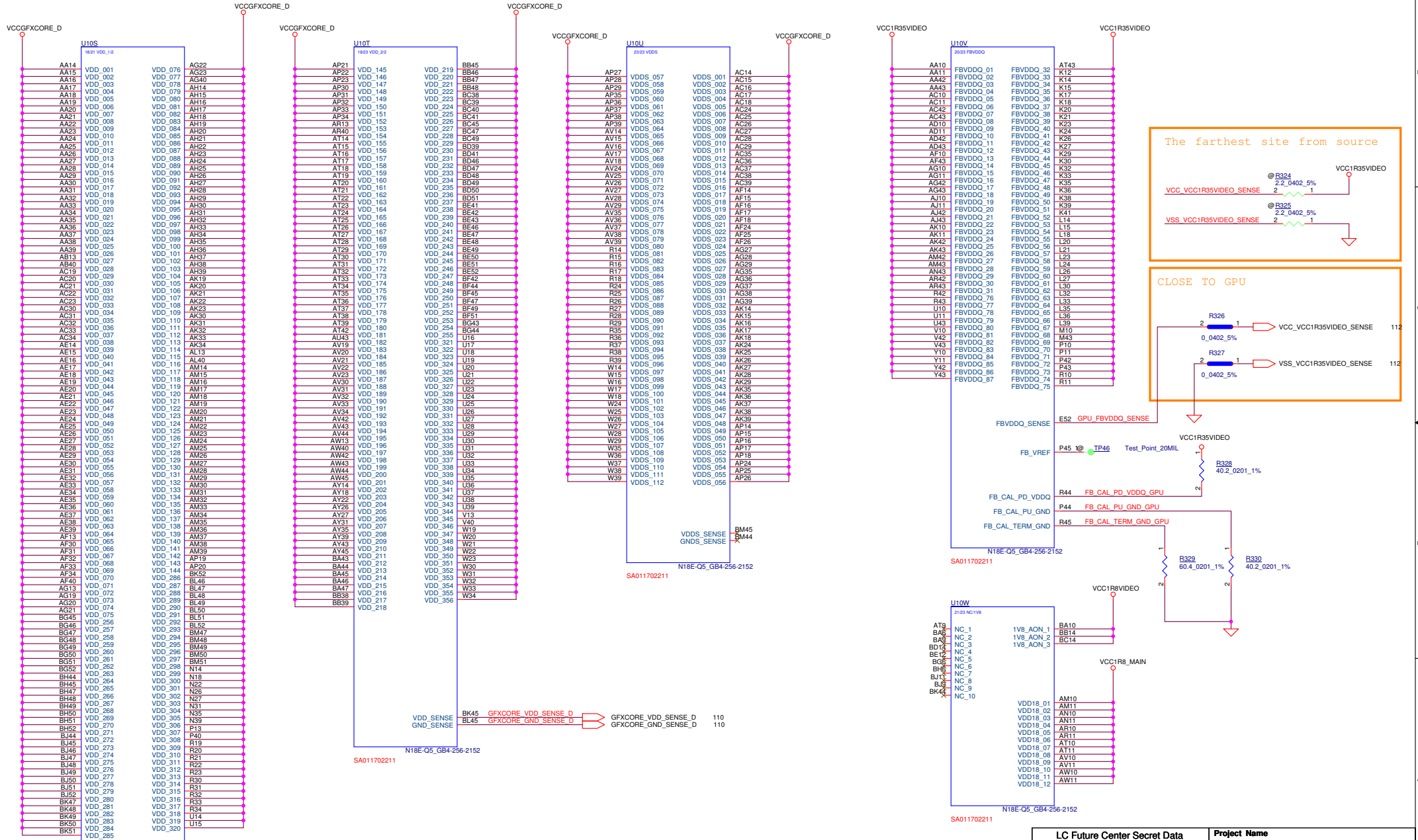


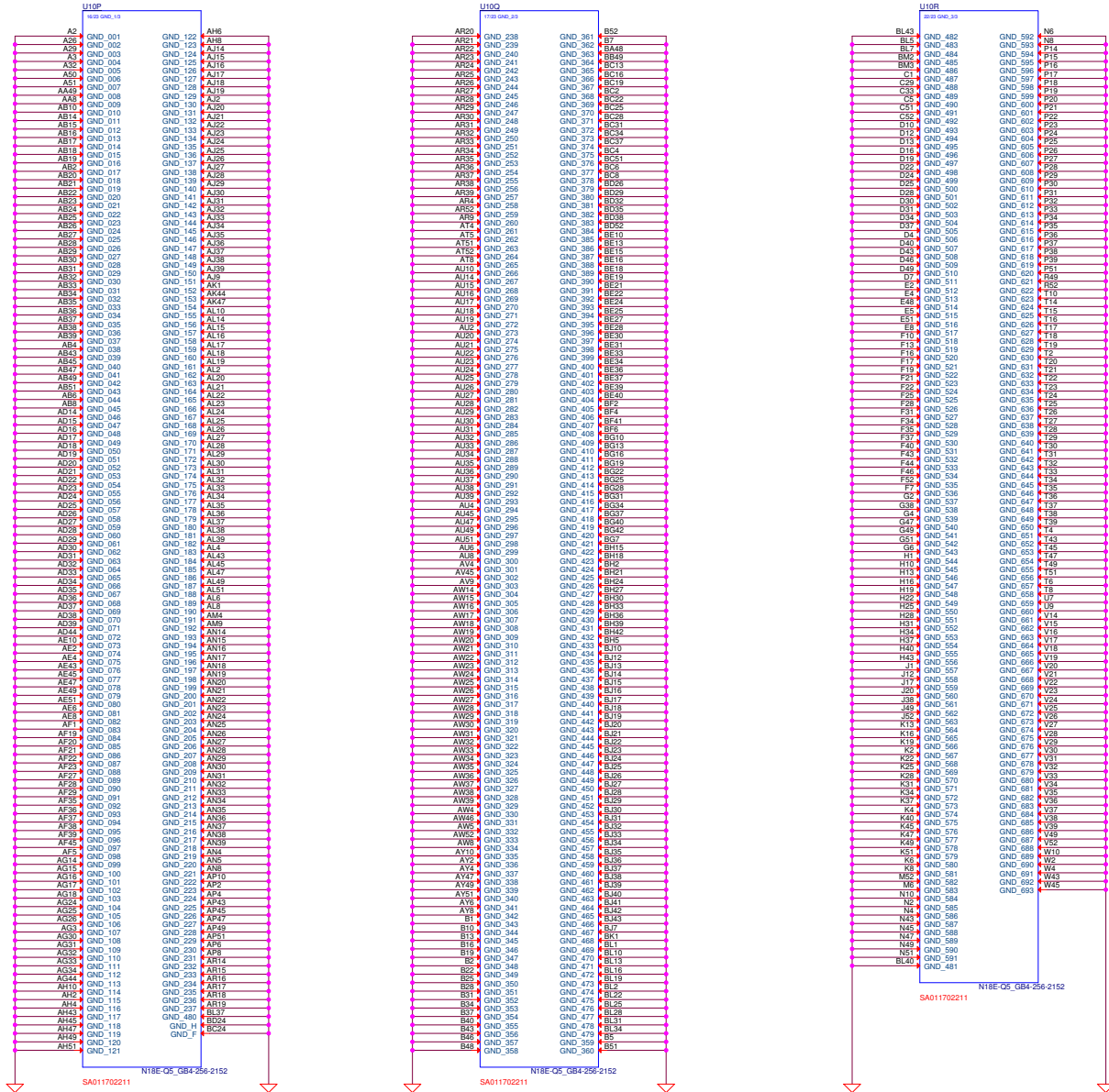
Vinafix.com

GPIO9	TEMP_ALERT*	I/O	Active Low Thermal Alert	Open Drain 10 k Ω pull-up to V18_A0N	GPIO24	GPU_PEX_RST_HOLD	control	10 k Ω pull-up to gated 3V3	NV_ask V18_A0N
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 k Ω pull-down	GPIO24	HPD_IPF*	i	Hot plug detect for IPFF	Inverted input. See Figure 14.5

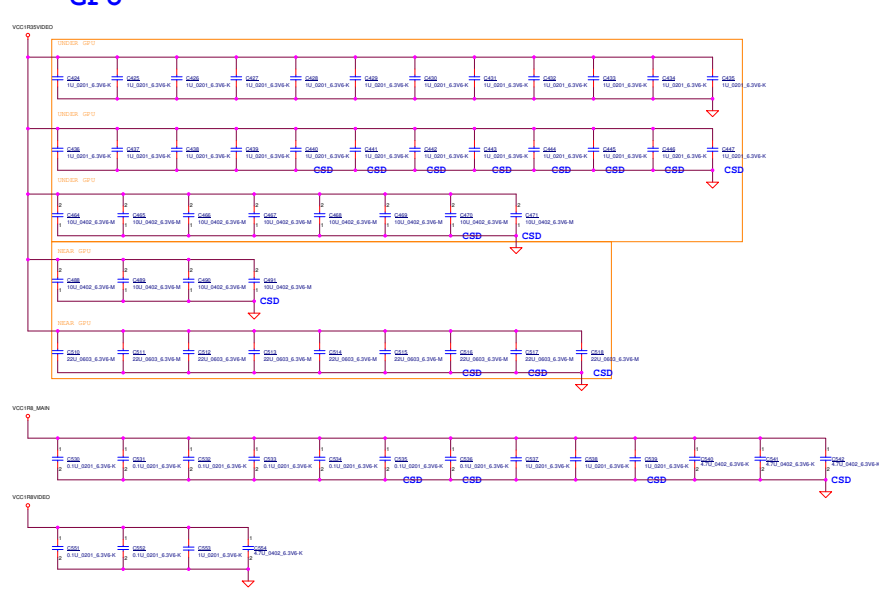


GPU

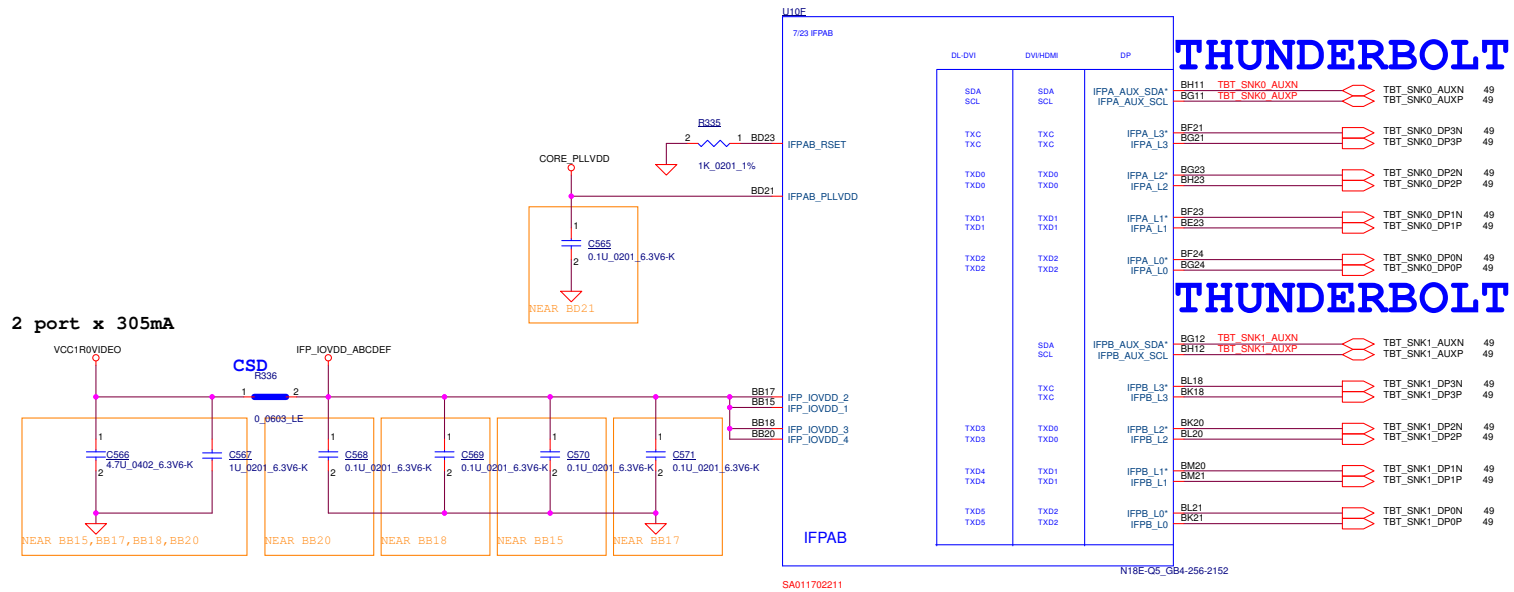
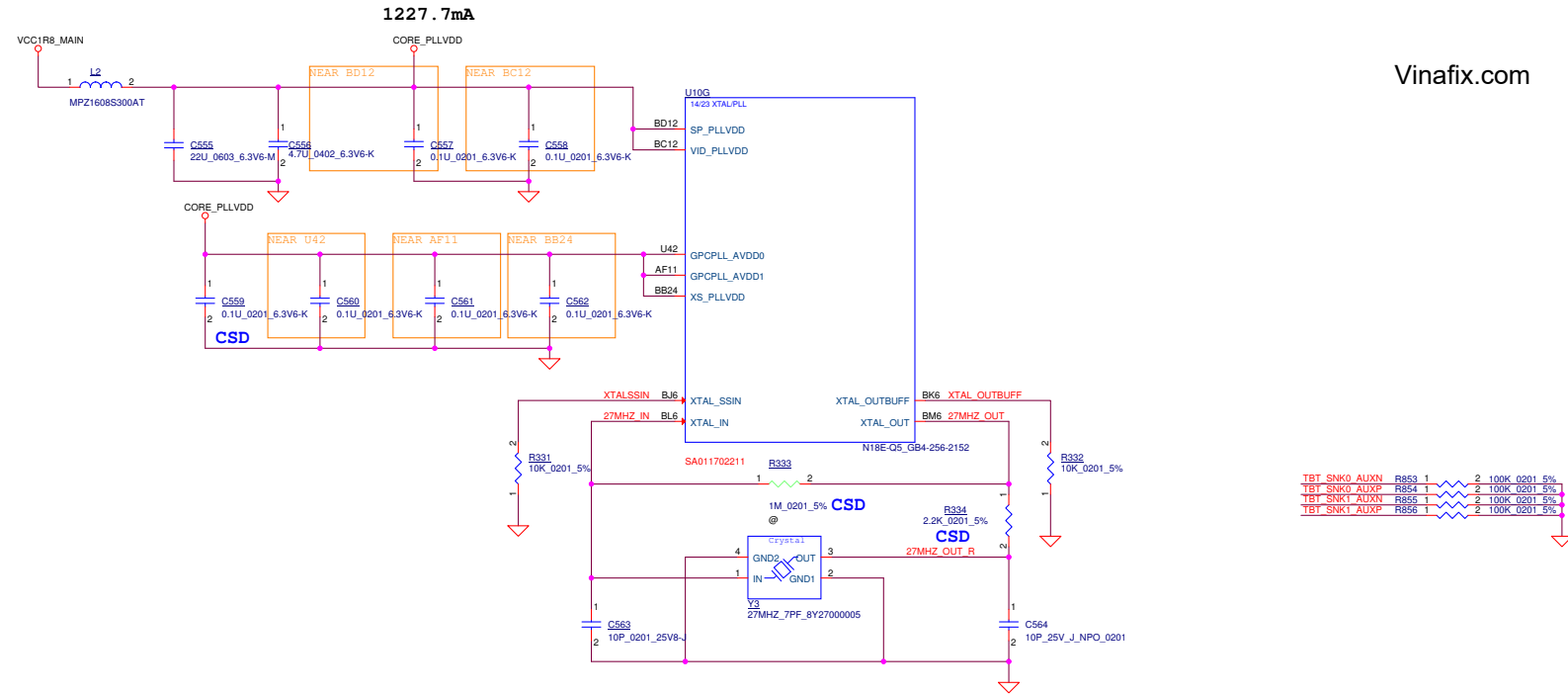




GPU

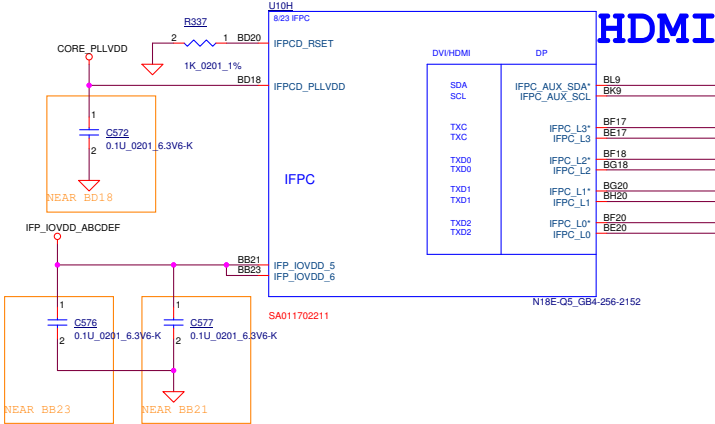


GPU

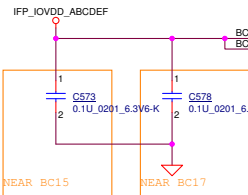


GPU

2 port x 305mA

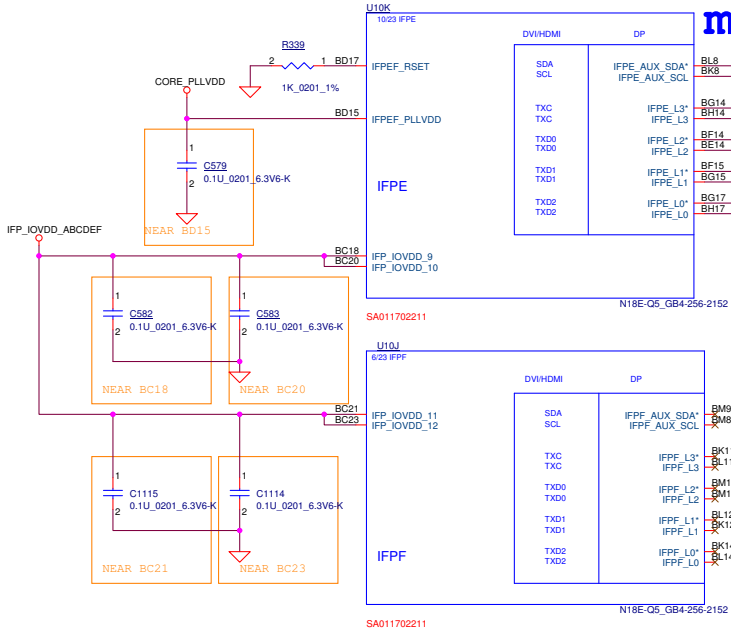


HDMI



PANEL

1 port x 305mA



mDP PORT

Close to U24

EDP_AUXN_D R904 1 2 100K 0201 5%

EDP_AUXP_D R905 1 2 100K 0201 5%

EXT_AUXN_GPU R906 1 2 100K 0201 5%

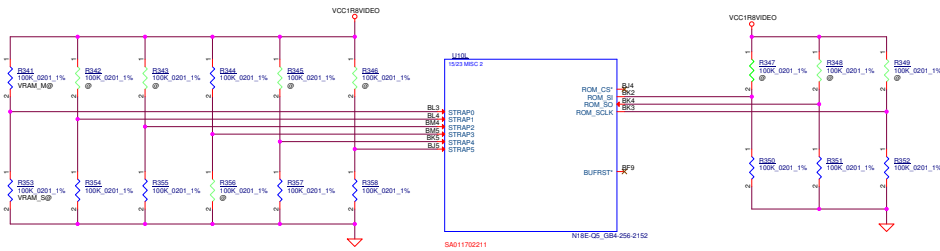
EXT_AUXP_GPU R907 1 2 100K 0201 5%

Close to C630, C631

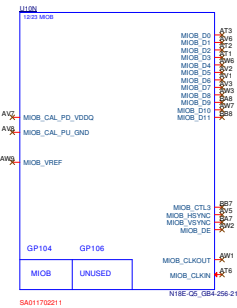
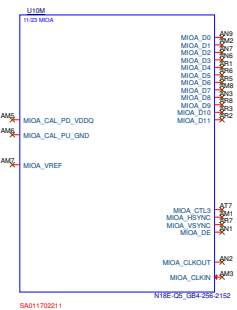
Table 10.1 Digital Display Link Summary

Digital Display Link	Dual-Link DVI	HDMI	DisplayPort
IFPA (Link A)	✓(Dual Link with IFPB)	✓	✓
IFPB (Link B)	✓(Dual Link with IFPA)	✓	✓
IFPC (Link C)	✓(Dual Link with IFPD)	✓	✓
IFPD (Link D)	(not supported)	(not supported)	eDP Only (no ext. display)
IFPE (Link E)	✓(Dual Link with IFPF)	✓	✓
IFPF (Link F)	✓(Dual Link with IFPE)	✓	✓

GPU



Strap0 table for VRAM vendor				
Vendor	R341	R353	LCFC P/N	
VRAM_S@	Samsung	NO ASM	100K 1%	SA000072710
VRAM_M@	Micron	100K 1%	NO ASM	SA000072910



- **SMB_ALT_ADDR Enable:** This strap function allows an alternate SMBus address to be configured, so that graphics circuits with multiple GPUs can have separate SMBus connections for each GPU. In dual GPU configurations, use of the alternate address on one GPU (by setting this function to '1') avoids conflicts between the two GPUs on an SMBUS port. The "SMB_ALT_ADDR disabled" setting ('0') is correct for single-GPU graphics circuits. (see Section 13.2.1 for the SMBus address.)
- **DEVID_SEL:** NVIDIA defines an original and a re-brand Device ID on a per-GPU basis. This Device ID Select strap function allows selection between the original PCIe Device ID defined for the GPU (via a function setting of '0'), and the alternate "re-brand" Device ID defined for the GPU (via a function setting of '1').
- **PCIE_CFG:** This function sets electrical characteristics of PCIe lanes, in particular signal amplitude (swing). A setting of '0' selects normal (full) signal swing. N17x graphics circuits should strap for this setting. (A setting of '1' designates reduced signal amplitude, available if special concerns require. Consult NVIDIA for guidance.)
- **VGA_DEVICE:** This strap function is used to report the graphics circuit either as a 3D device (class code 302, designated by a setting of '0' for this strap) or as a VGA device (class code 300, designated by a setting of '1') to the host system. The 3D Device (class code 302, strap='0') setting is correct for most MS-Hybrid notebook GeForce graphics circuits.

Table 5.3 RAMCFG

Strap Pins <small>see Note</small>			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)
M	H	L	14 (0x000E)
M	H	H	15 (0x000F)
H	L	M	16 (0x0010)
H	M	L	17 (0x0011)
H	M	H	18 (0x0012)
H	H	M	19 (0x0013)
L	M	M	20 (0x0014)
M	L	M	21 (0x0015)
M	M	L	22 (0x0016)
M	M	H	23 (0x0017)
M	H	M	24 (0x0018)
H	M	M	25 (0x0019)
M	M	M	26 (0x001A)

Note: The ternary strap pins listed in the STRAP columns must be pulled to one of three voltage levels. "L" means Low level (GND). "M" means middle level (0.9V). "H" means High level (1.8V).

Table 5.4 Display Link to SORx_EXPOSED Mapping for Down Designs

Total Display Links (HDMI, DP or DVI)			See This Row of Table 5.5
	Total Enabled for Audio (HDMI, DP or DVI)		
	Is IFPD used? (Only supports eDP.)		
4	4	NO	15
4	3	YES	13
3	3	NO	14
3	2	YES	12
2	2	NO	12
2	1	YES	8
1		NO	8
1	0	YES	0
No other configurations are supported.			

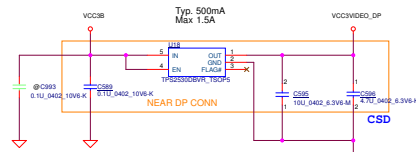
Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins <small>see Note</small>			Resulting SORx_EXPOSED Enablements			
	ROM_SD	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
M	X	X	X	(Reserved; do not configure)			
All other Strap Configurations				(Reserved)			

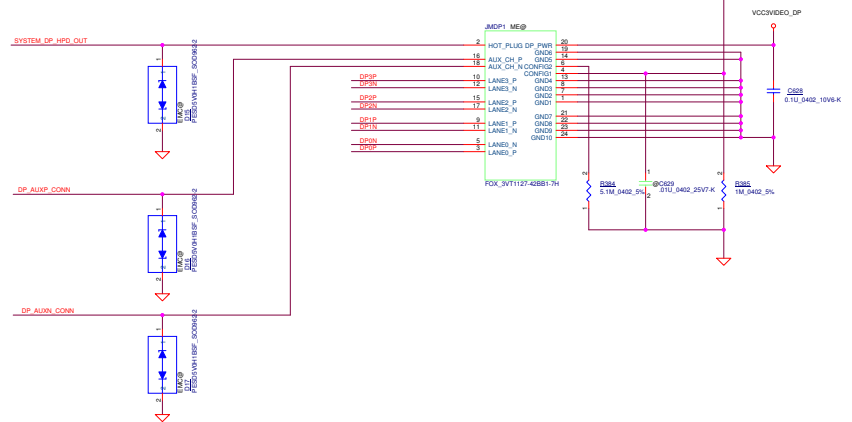
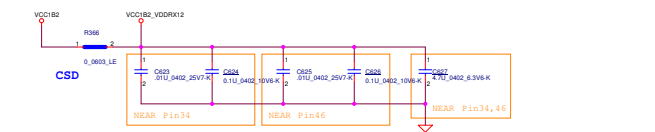
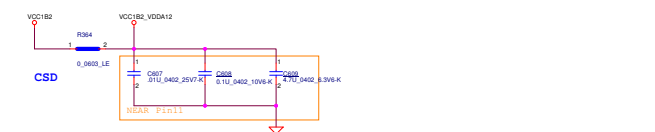
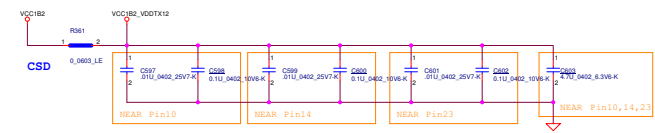
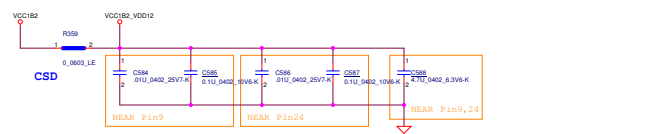
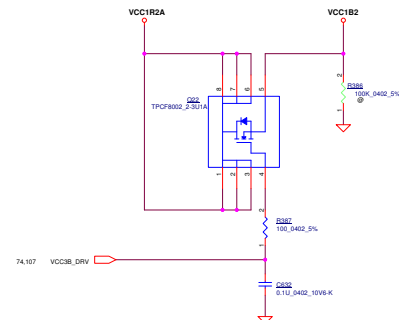
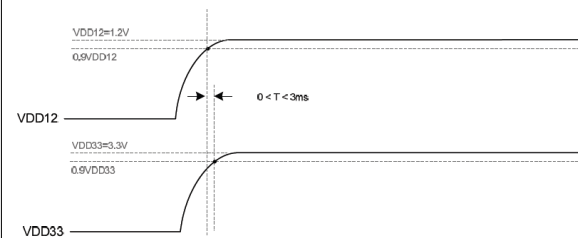
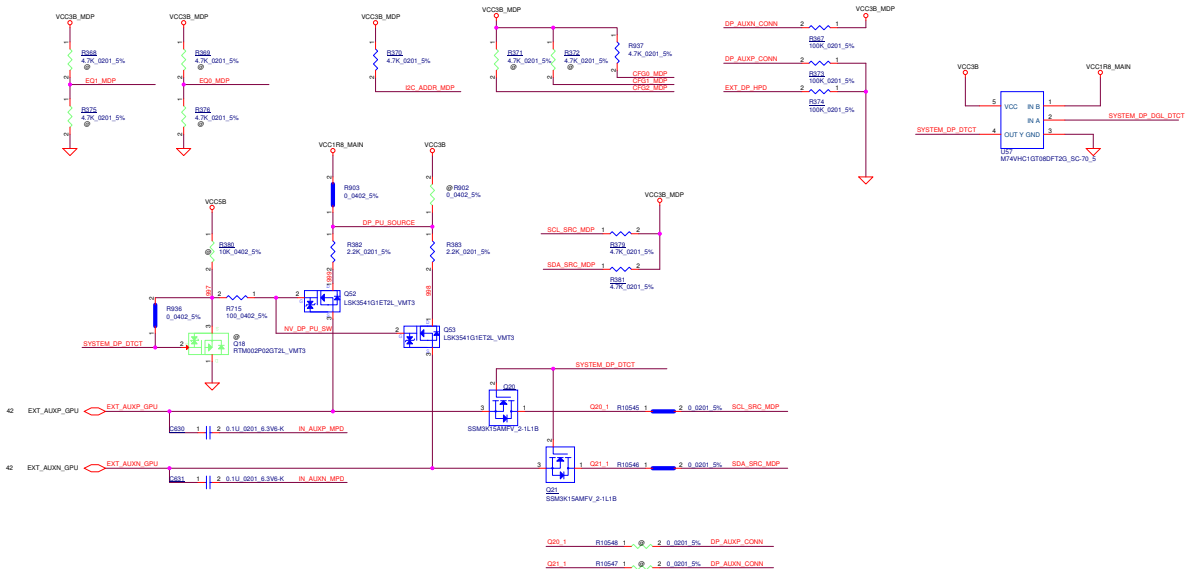
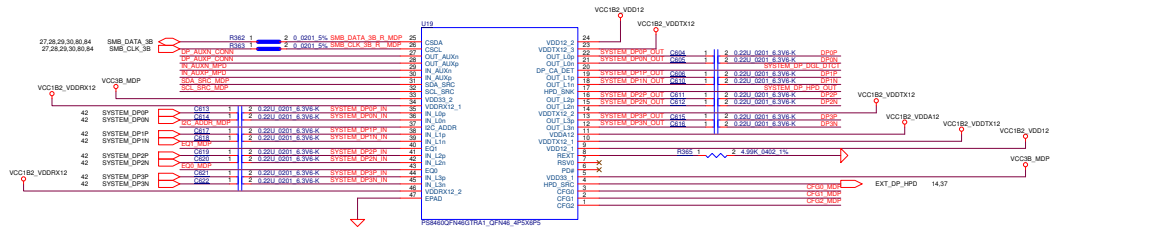
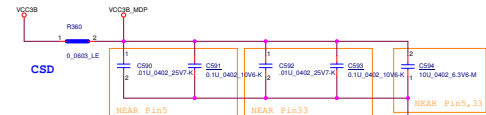
Table 5.6 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins <small>Note 1</small>			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1
H	L	M	Reserved			
H	M	L				
H	M	H				
H	H	M				
L	M	M				
M	L	M				
M	M	L				
M	M	H				
M	H	M				
H	M	M				

MINI DISPLAY PORT

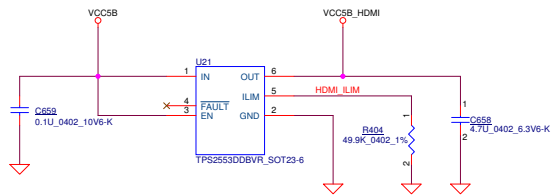
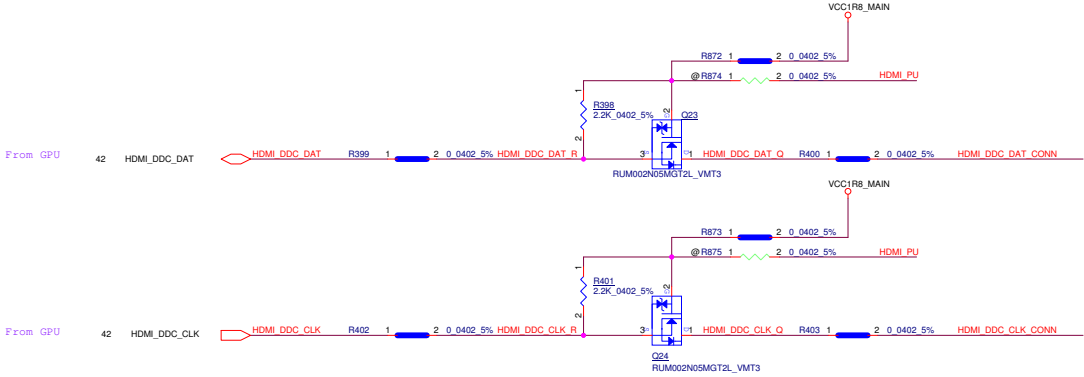
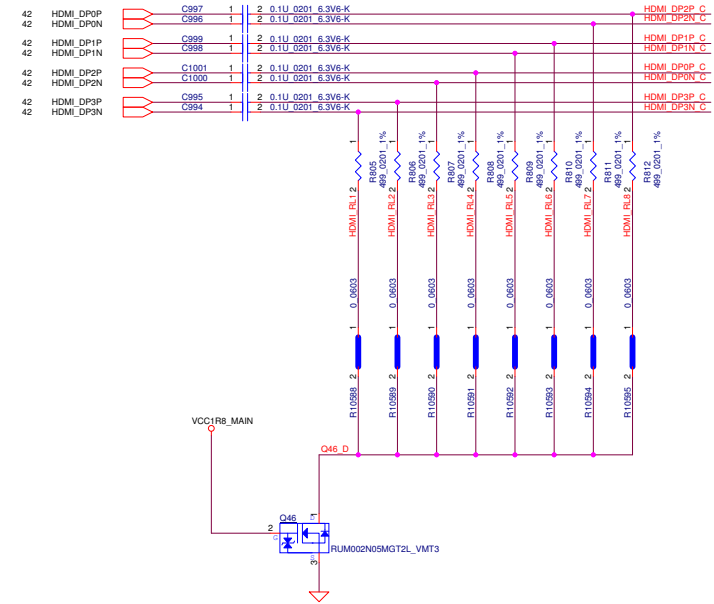
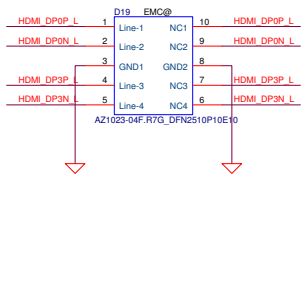
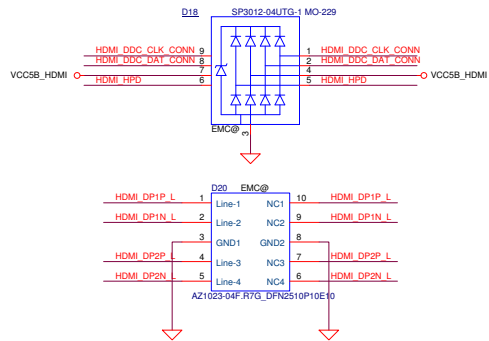


Vendor	P/N
TI	TPS2530DBVR (SA00005R000)
On-semi	NCP380HSN05AAT1G (SA00005OV00)

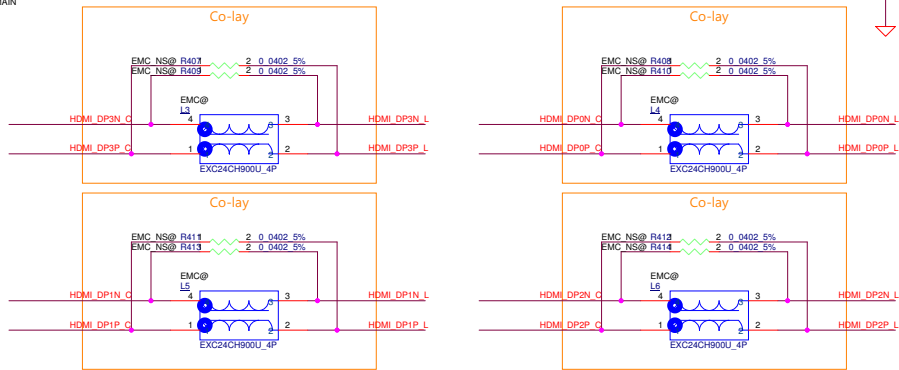
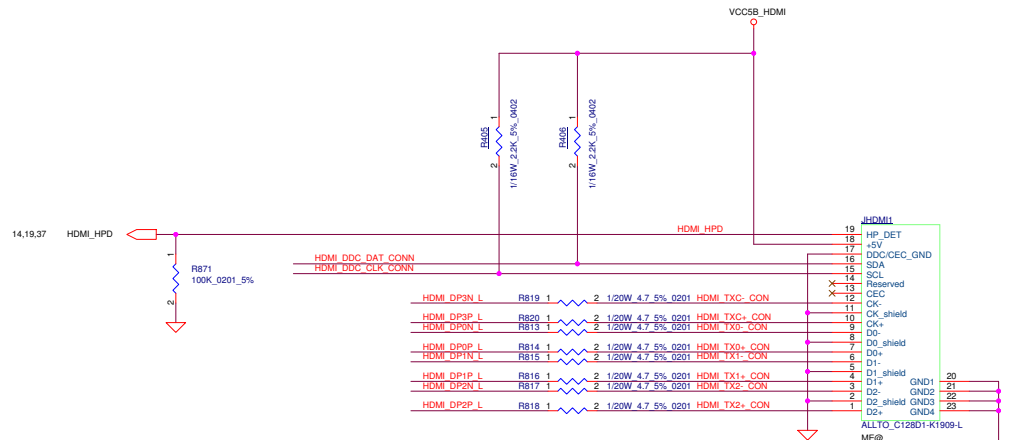


BLANK

HDMI



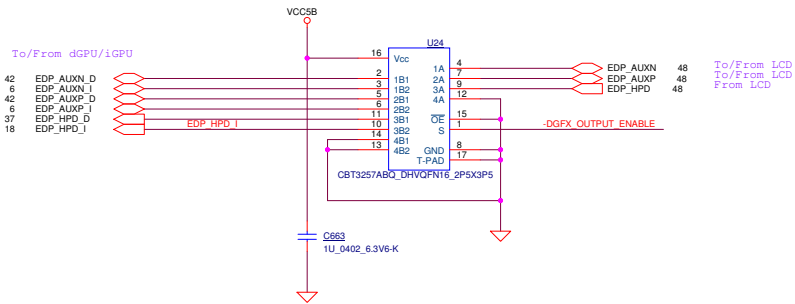
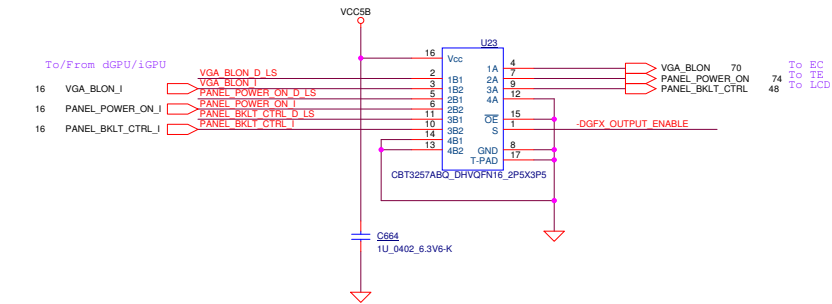
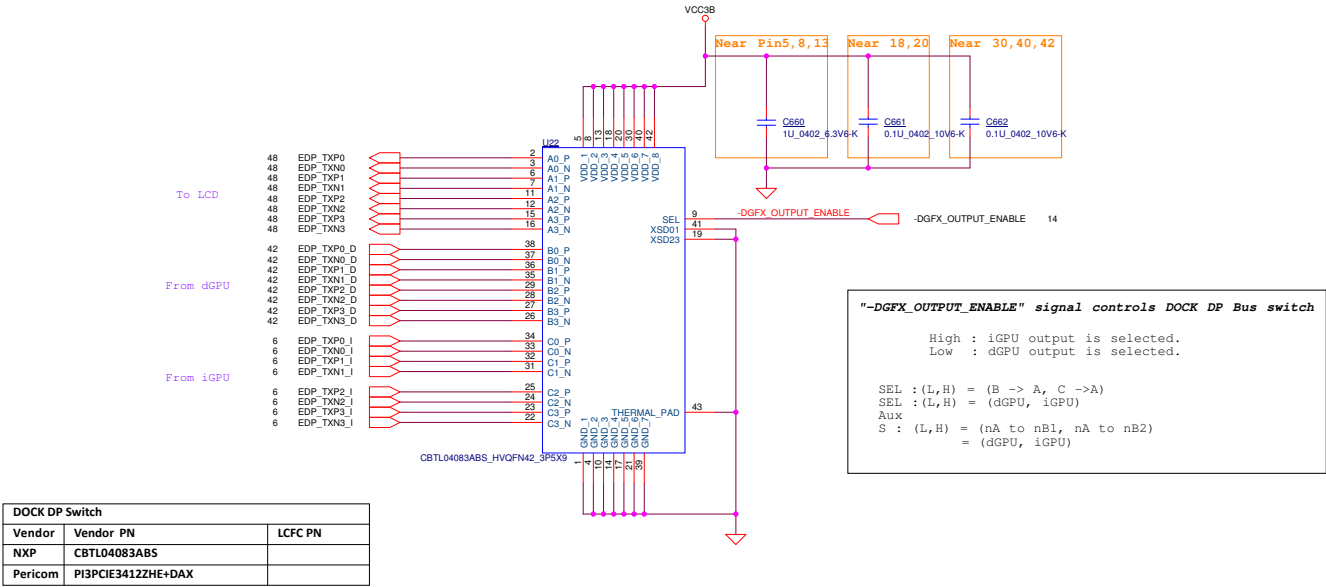
SDV & FVT will use SD03459028J(59K_0402_1%)
SIT will use SA000073T00 (61.9K_0402_1%)



HDMI_TXC+ CON	R10607	1	@	2	1/20W 150.5% 0201	HDMI_TXC+ CON
HDMI_TX0+ CON	R10608	1	@	2	1/20W 150.5% 0201	HDMI_TX0+ CON
HDMI_TX1+ CON	R10609	1	@	2	1/20W 150.5% 0201	HDMI_TX1+ CON
HDMI_TX2+ CON	R10610	1	@	2	1/20W 150.5% 0201	HDMI_TX2+ CON

eDP DEMUX

Vinafix.com

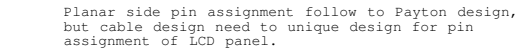


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But Footprint :SA00003R00J
MC74VHC1GT08

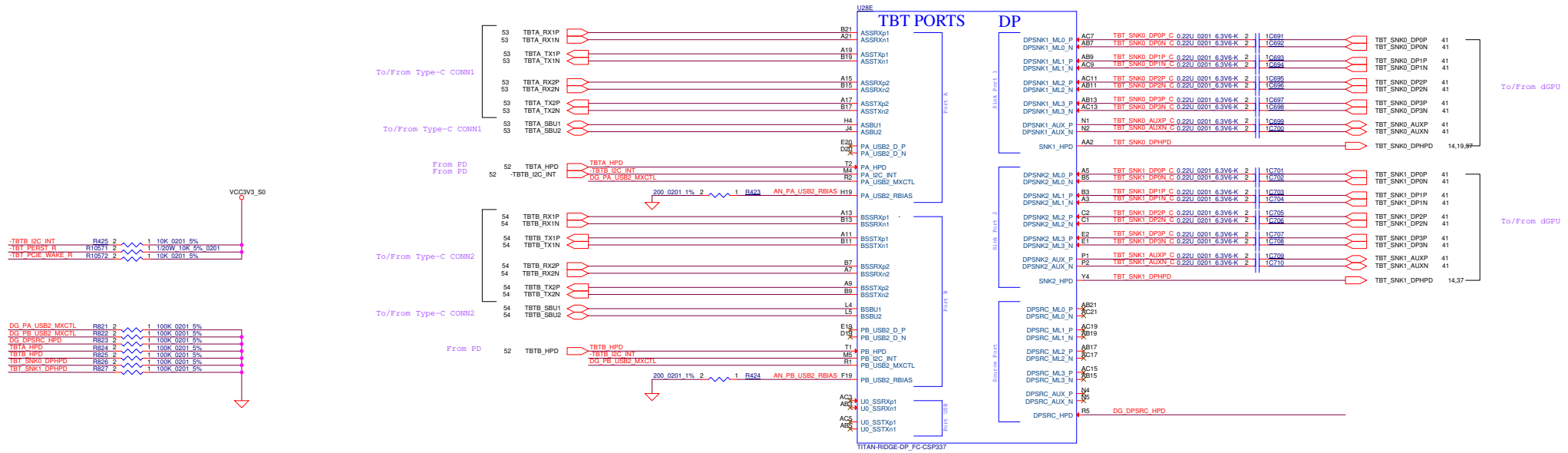
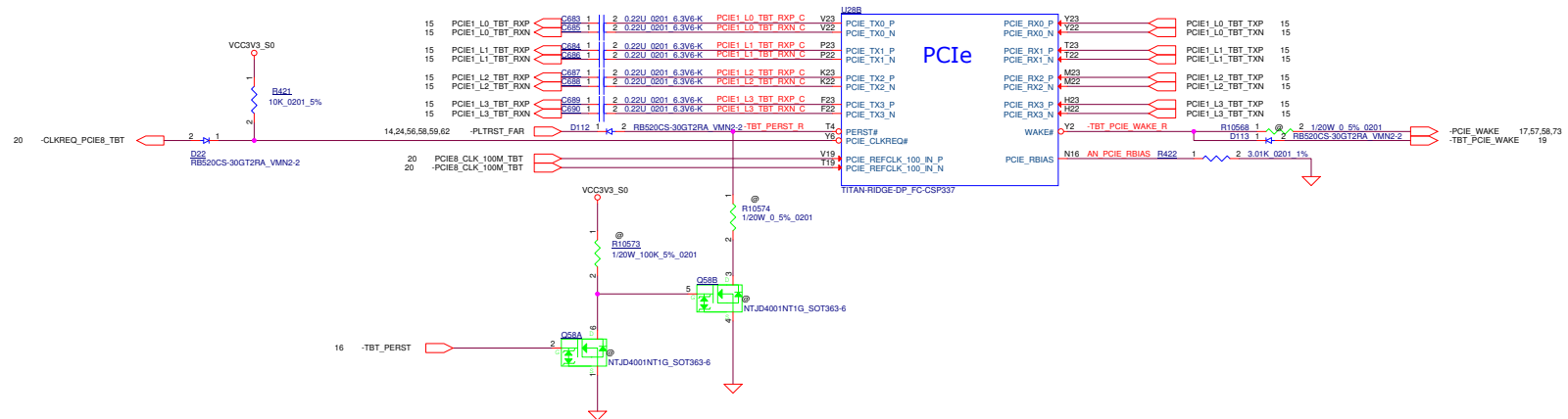


PANEL_BKLT_CTRL_I R857 1 2 100K 0201 5%
VGA_BLOK_I R858 1 2 100K 0201 5%
PANEL_POWER_ON_I R859 1 2 100K 0201 5%
EDP_HPDI R860 1 2 100K 0201 5%

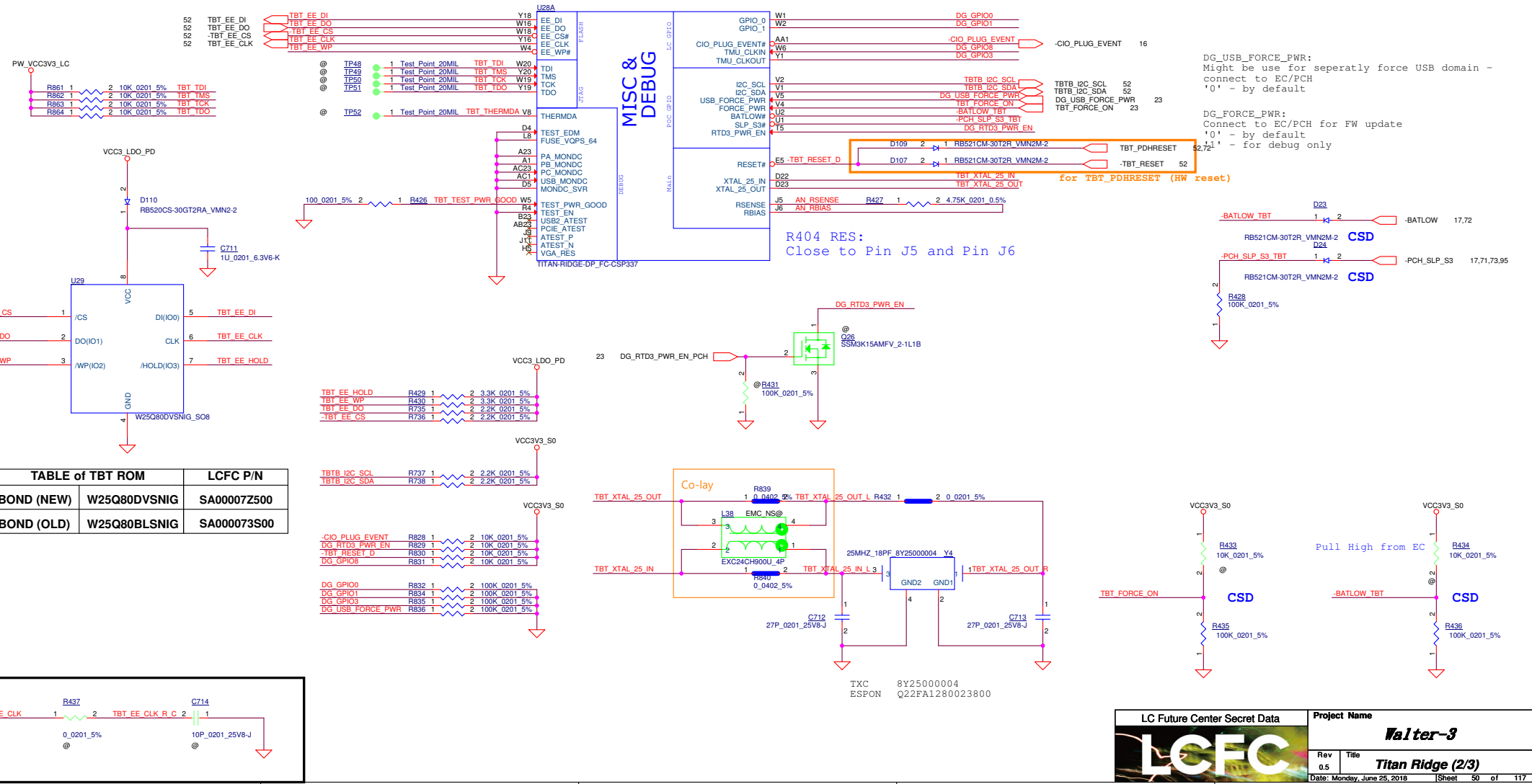
5	4	3	2	1
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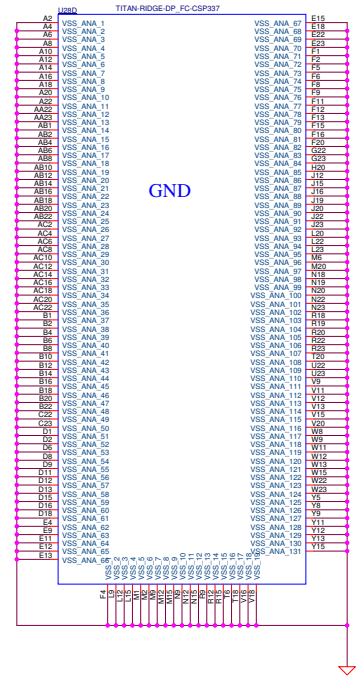
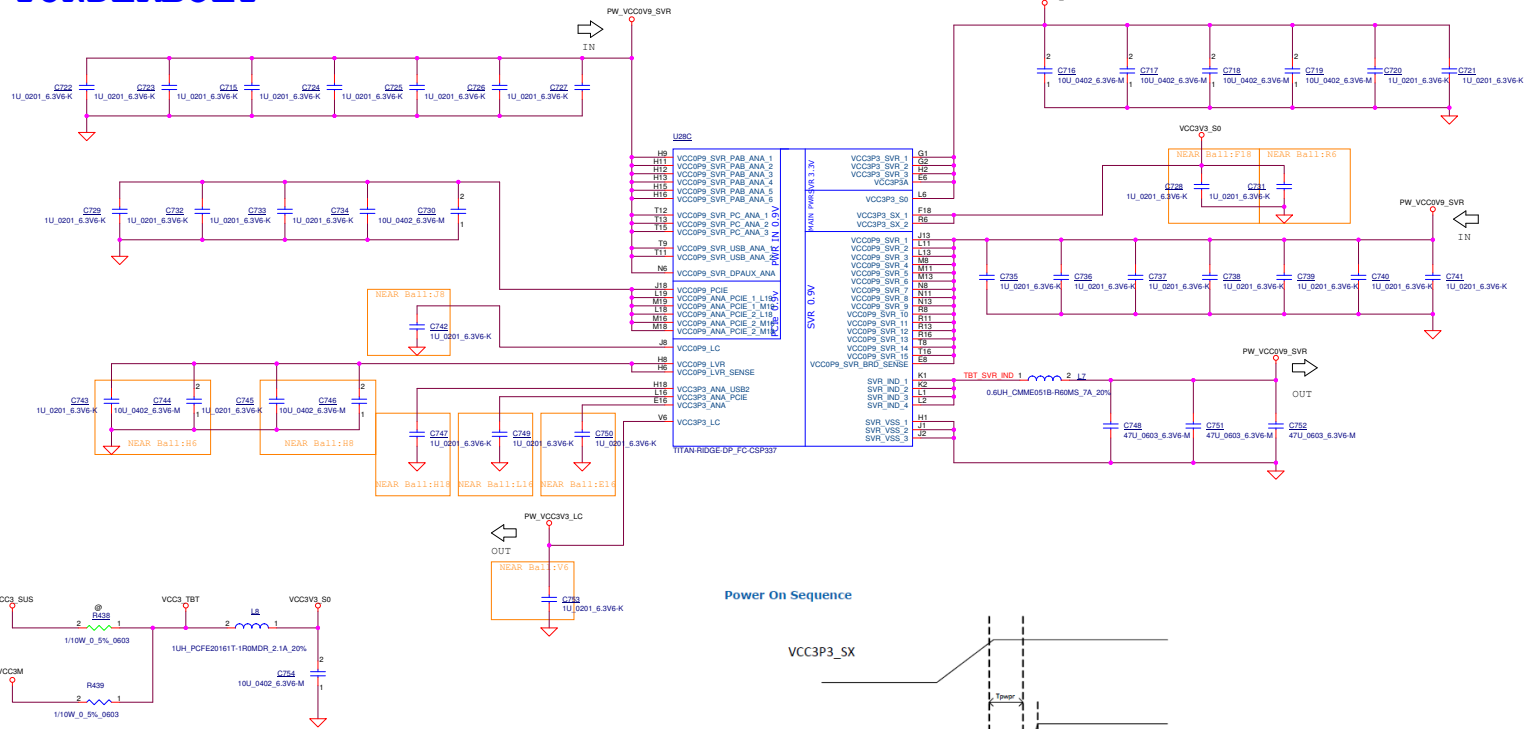
TUNDEBOLT



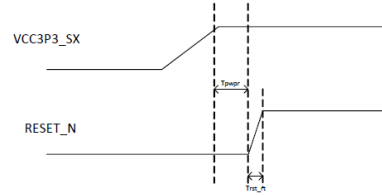
TUNDEBOLT



TUNDEBOLT



Power On Sequence



Power On Sequence

Parameter	Description	Min	Max	Units	Comments
Tpwpr	From VCC3P3_SX at 90% to RESET_N de-assertion	100	-	us	
Trst_rt	RESET_N rise time	0.1	500	ns	

POWER DELIVERY

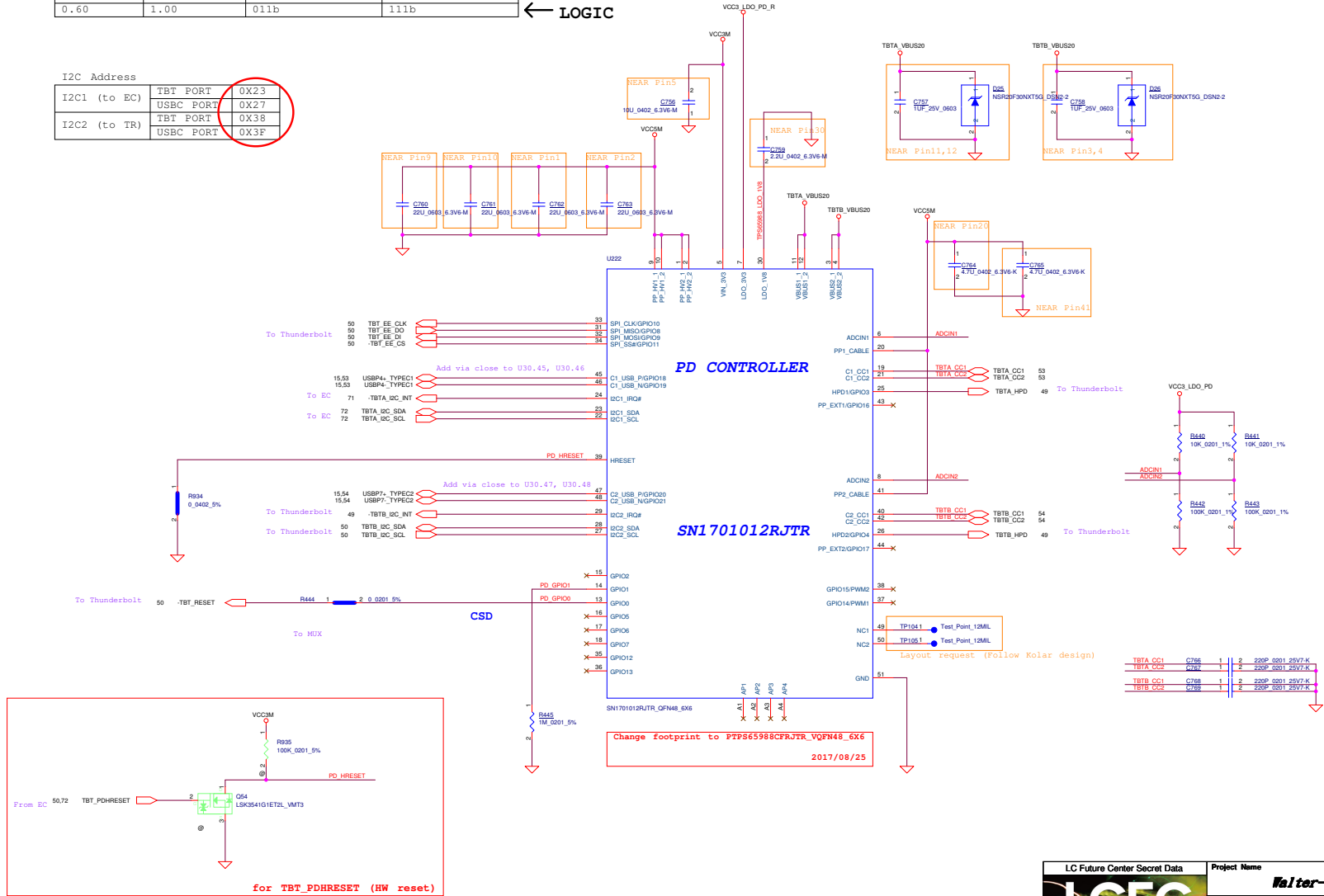
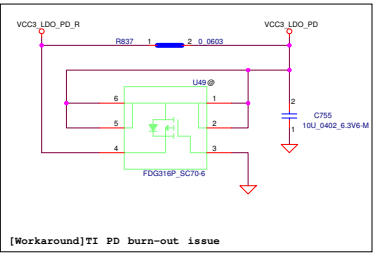
ADCIN1 BUS POWER CONFIGURATION		
DIV = PDR3 / (PDR1 + PDR3)		
DIV MIN	DIV MAX	CONFIGURATION
0.00	0.18	BP_NoResponse
0.20	0.38	BP_WaitFor3V3_Internal
0.40	0.58	BP_WaitFor3V3_External
0.60	1.00	BP_NoWait

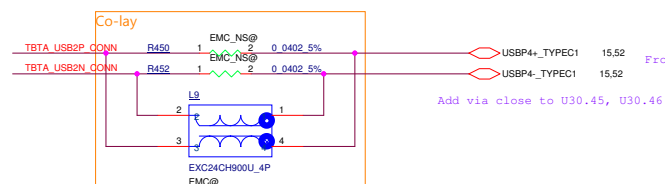
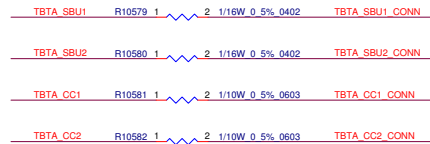
← LOGIC

ADCIN2 I2C Address Setting			
DIV = PDR4 / (PDR2 + PDR4)			
DIV MIN	DIV MAX	I2C Unique Address [3:1]	
DIV MIN	DIV MAX	ADC_ADDR_DECODE_C1	ADC_ADDR_DECODE_C2
0.00	0.18	000b	100b
0.20	0.38	001b	101b
0.40	0.58	010b	110b
0.60	1.00	011b	111b

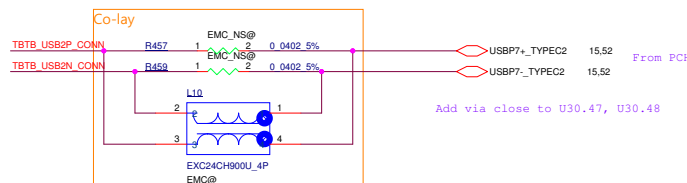
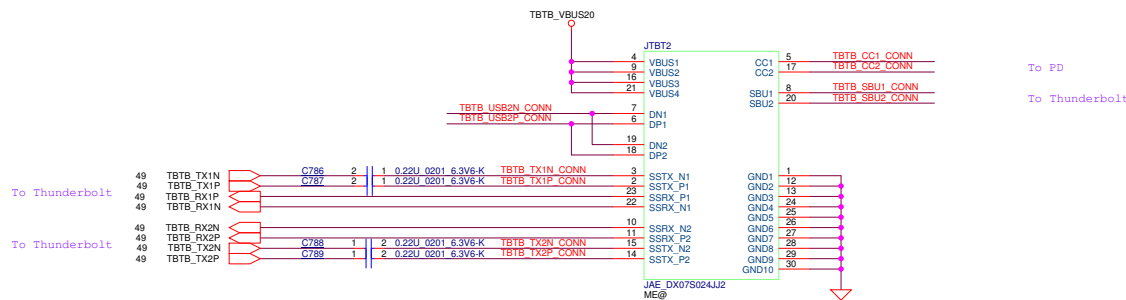
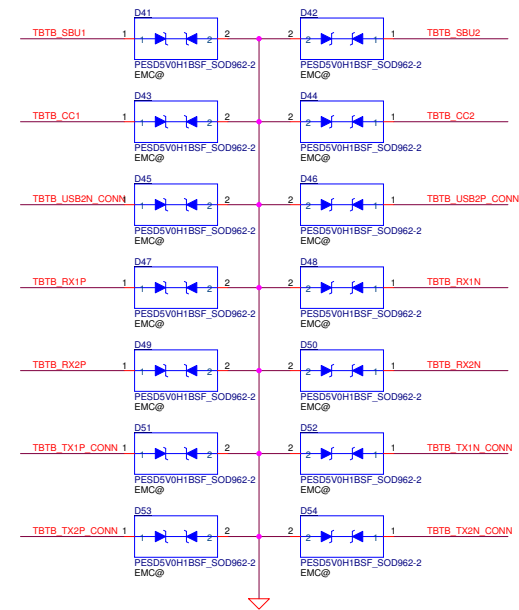
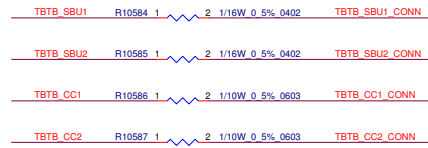
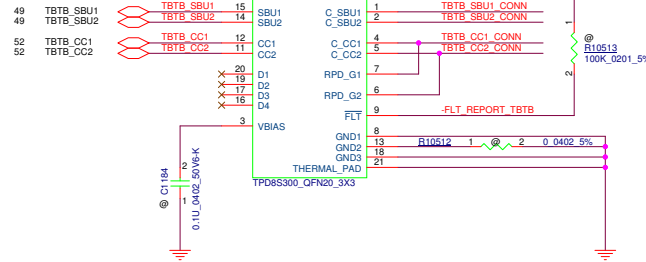
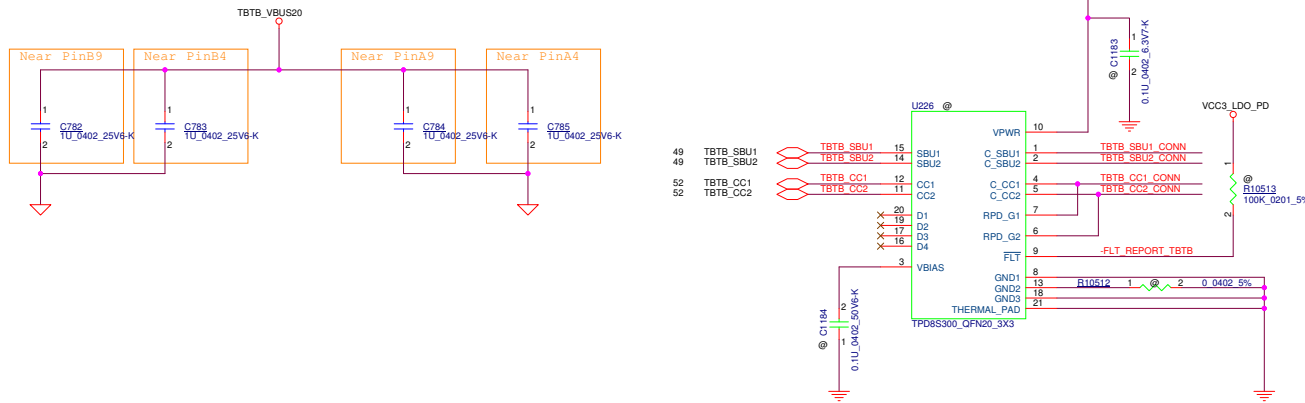
← LOGIC

I2C Address		
I2C1 (to EC)	TBT PORT	0X23
	USBC PORT	0X27
I2C2 (to TR)	TBT PORT	0X38
	USBC PORT	0X3F

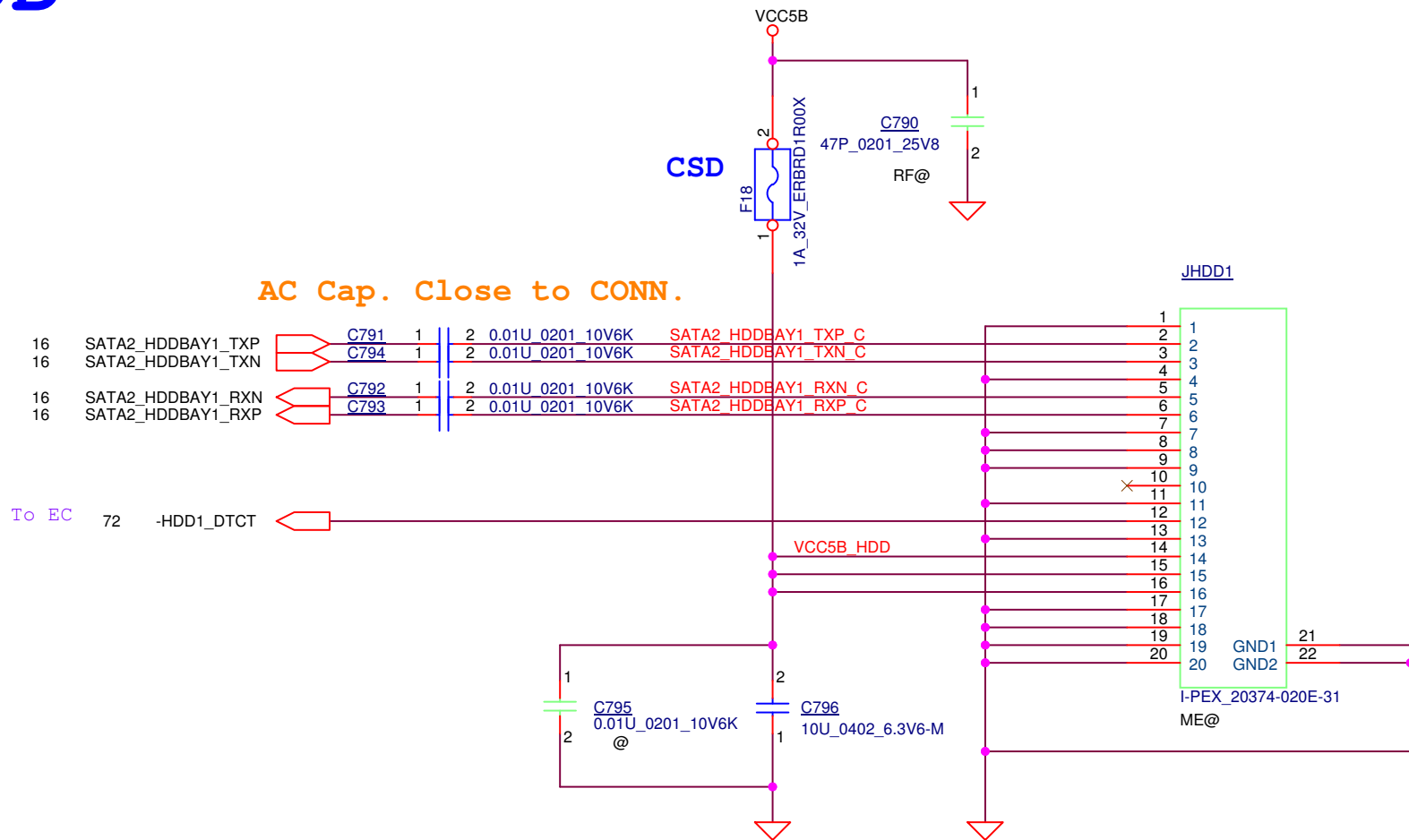




USB TYPE-C CONN 2



HDD



LC Future Center Secret Data



Project Name

Walter-3

Rev
0.5

Title

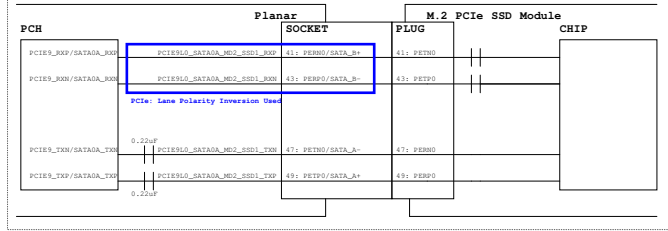
SATA HDD CONN

Date: Monday, June 25, 2018

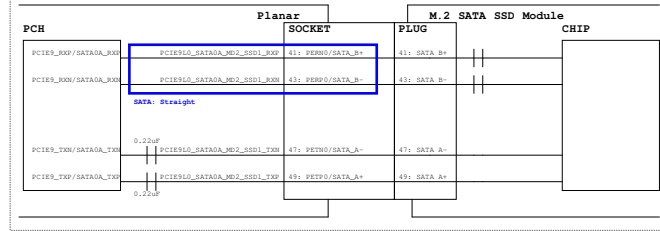
Sheet 55 of 117

M.2 SSD

M.2 PCIe SSD



M.2 SATA SSD



M.2 SSD slot 1 Type-M 2280

M.2 SSD slot 2 Type-M 2280

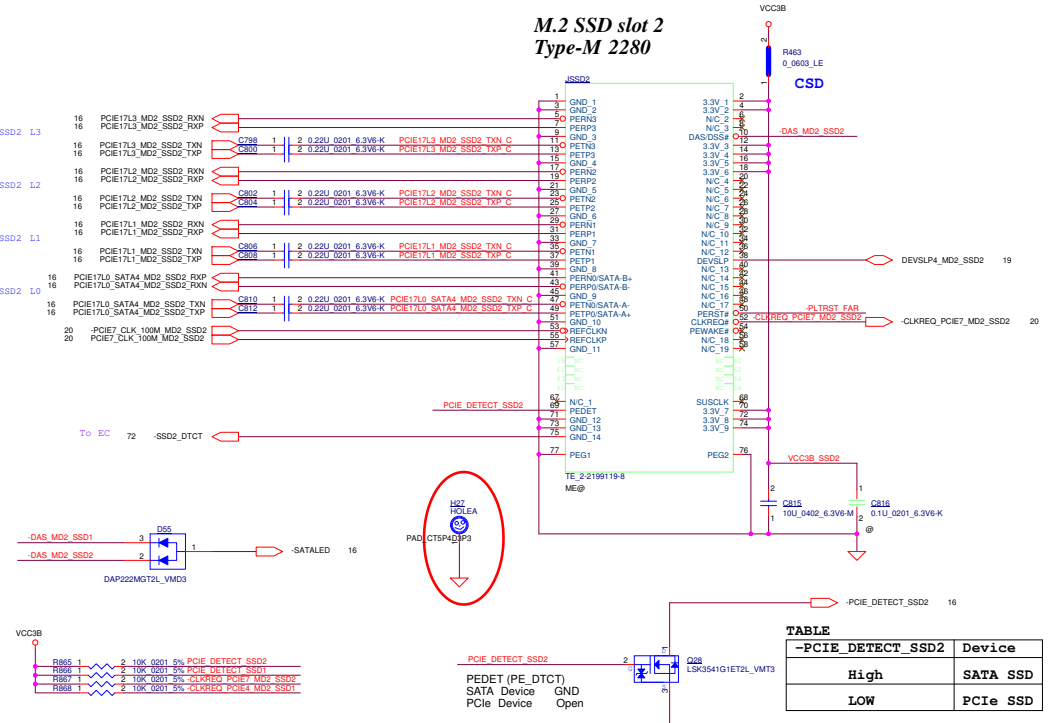
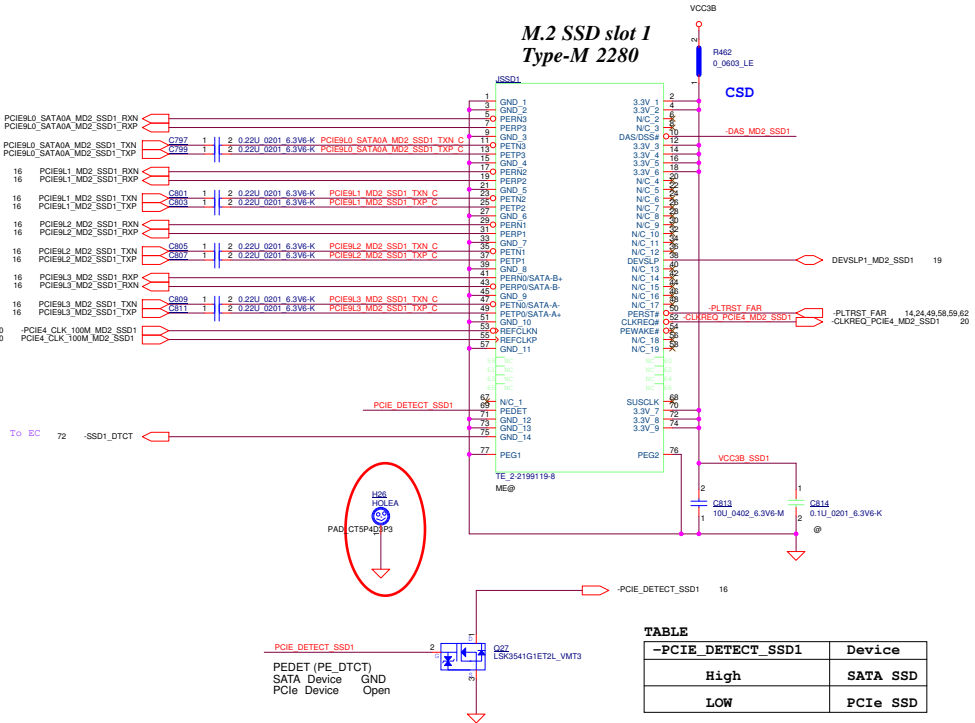


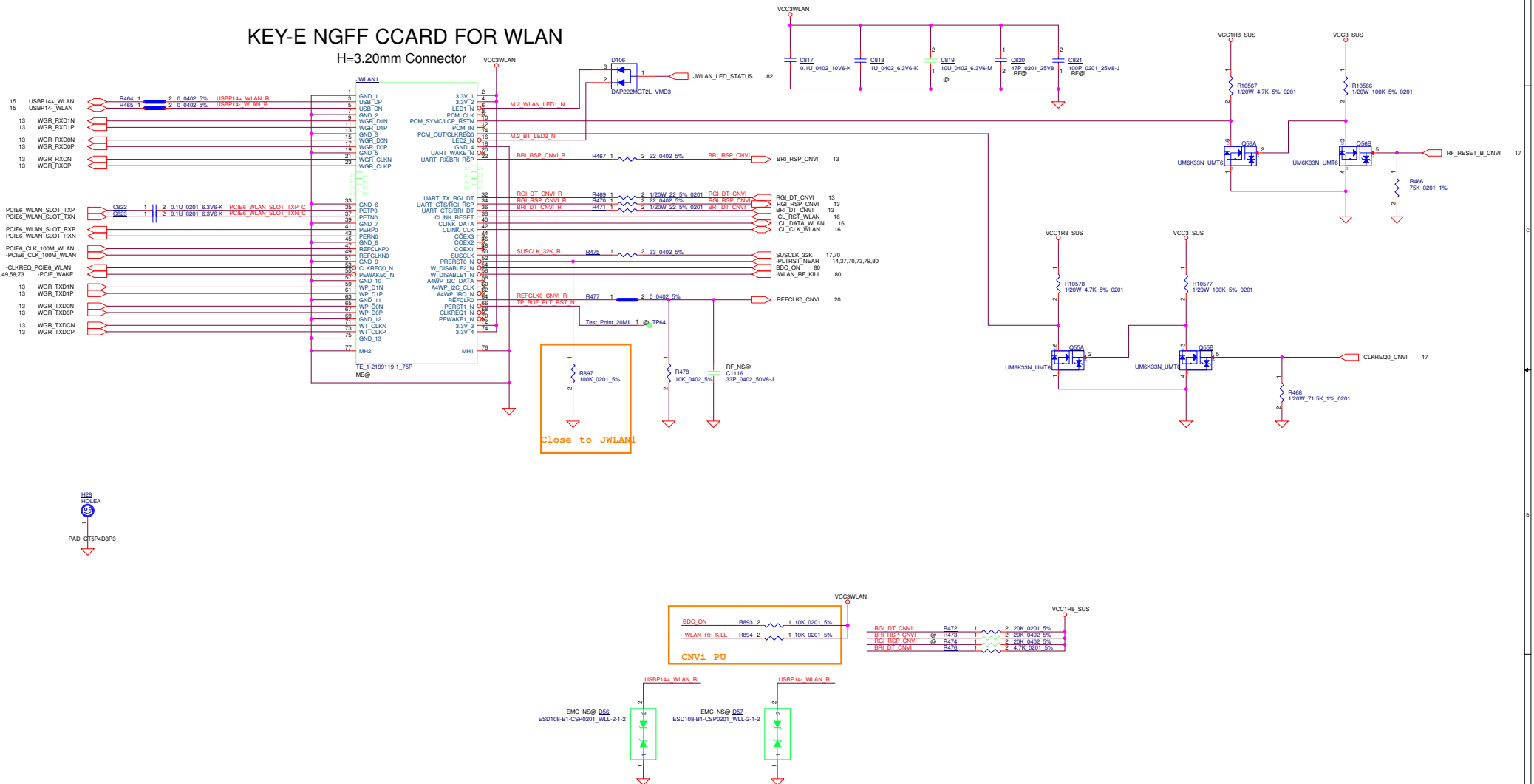
TABLE	
-PCIE_DETECT_SSD1	Device
High	SATA SSD
Low	PCIe SSD

TABLE	
-PCIE_DETECT_SSD2	Device
High	SATA SSD
Low	PCIe SSD

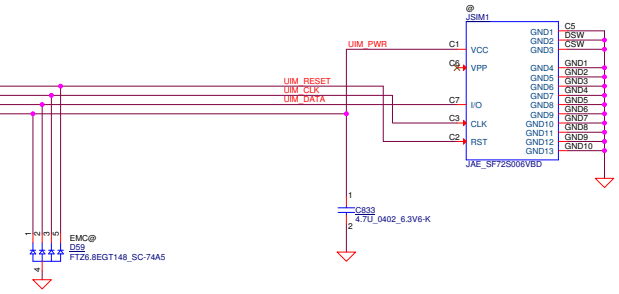
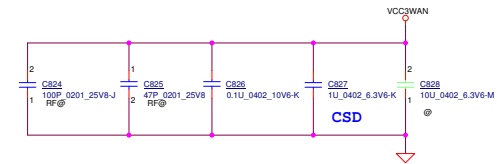
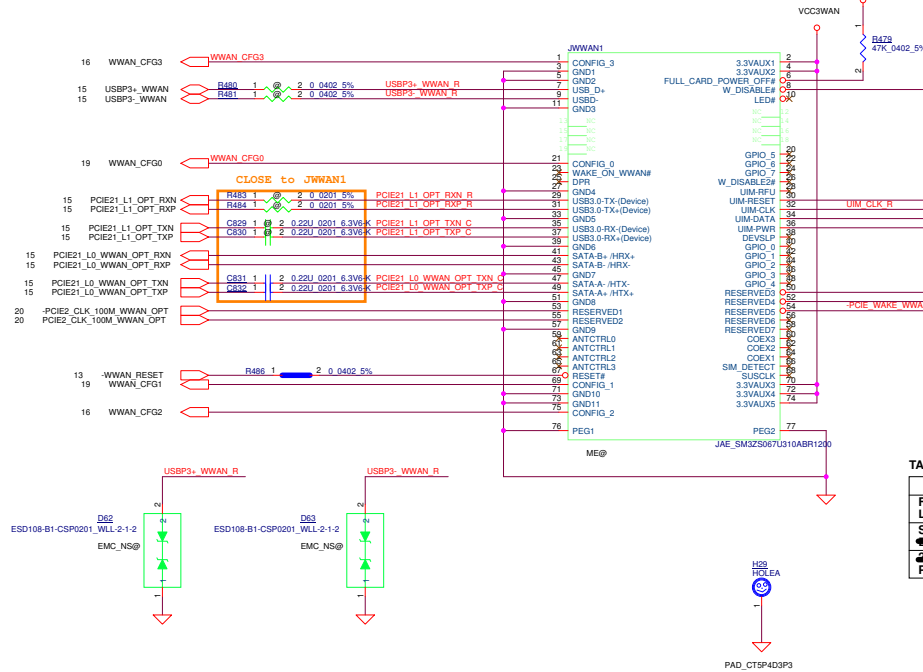
WLAN

KEY-E NGFF CCARD FOR WLAN

H=3.20mm Connector



M.2 Socket 2 (Key-B) for 3042 S3 WWAN
H=2.00mm Connector

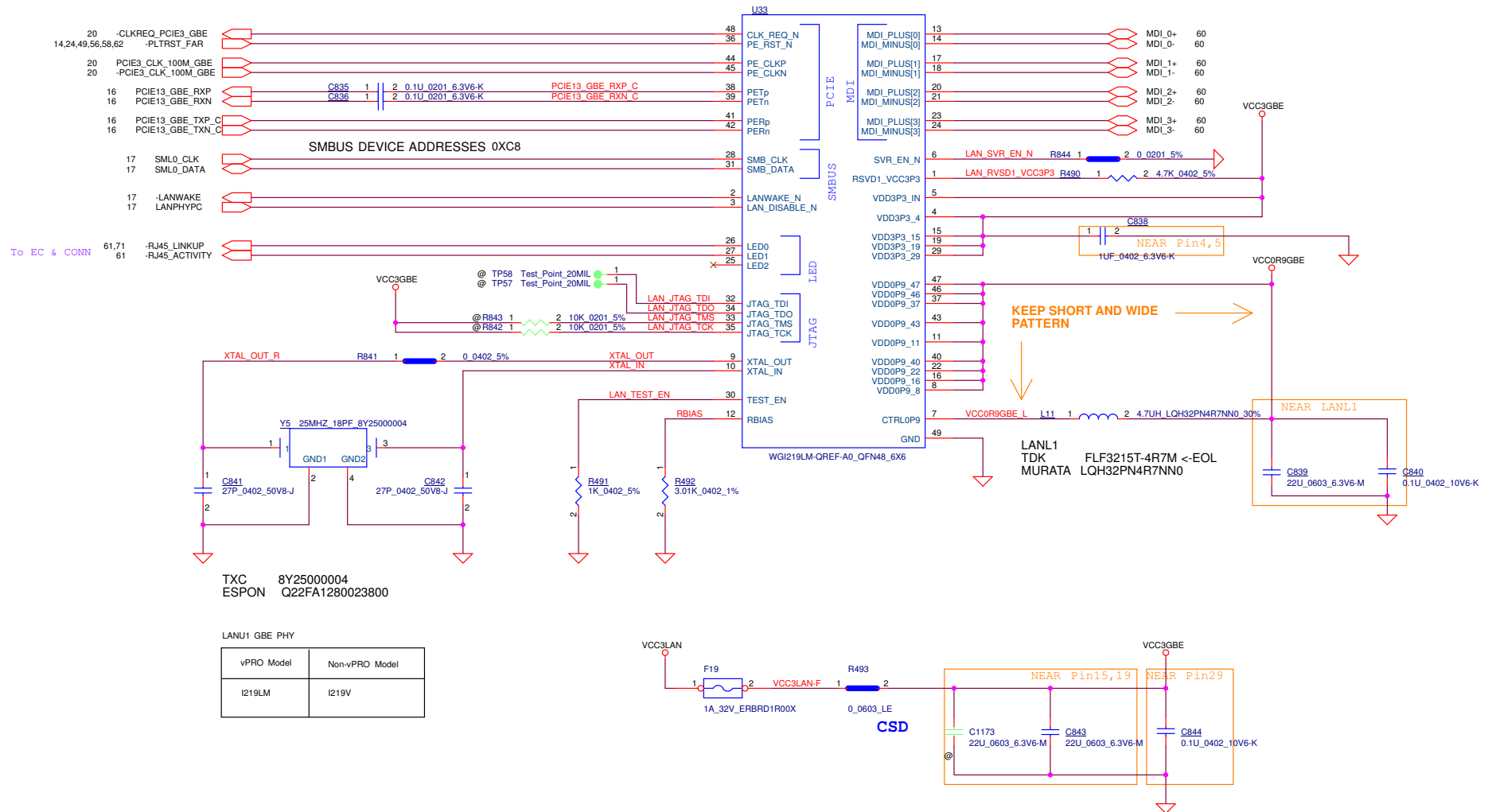


TABLE

	CONFIG 0	CONFIG 3	CONFIG 2	CONFIG 1
Fibocom L850-EB	GND	N.C.	GND	GND
Sierra EMR335	GND	N.C.	N.C.	GND
2242 SSD				
PCIe	GND	GND	GND	N.C.

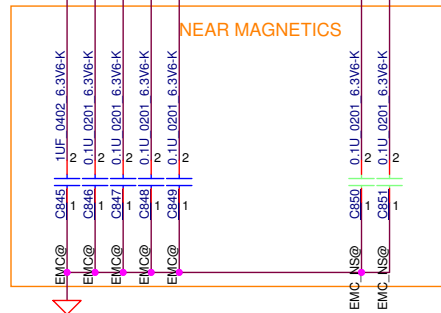
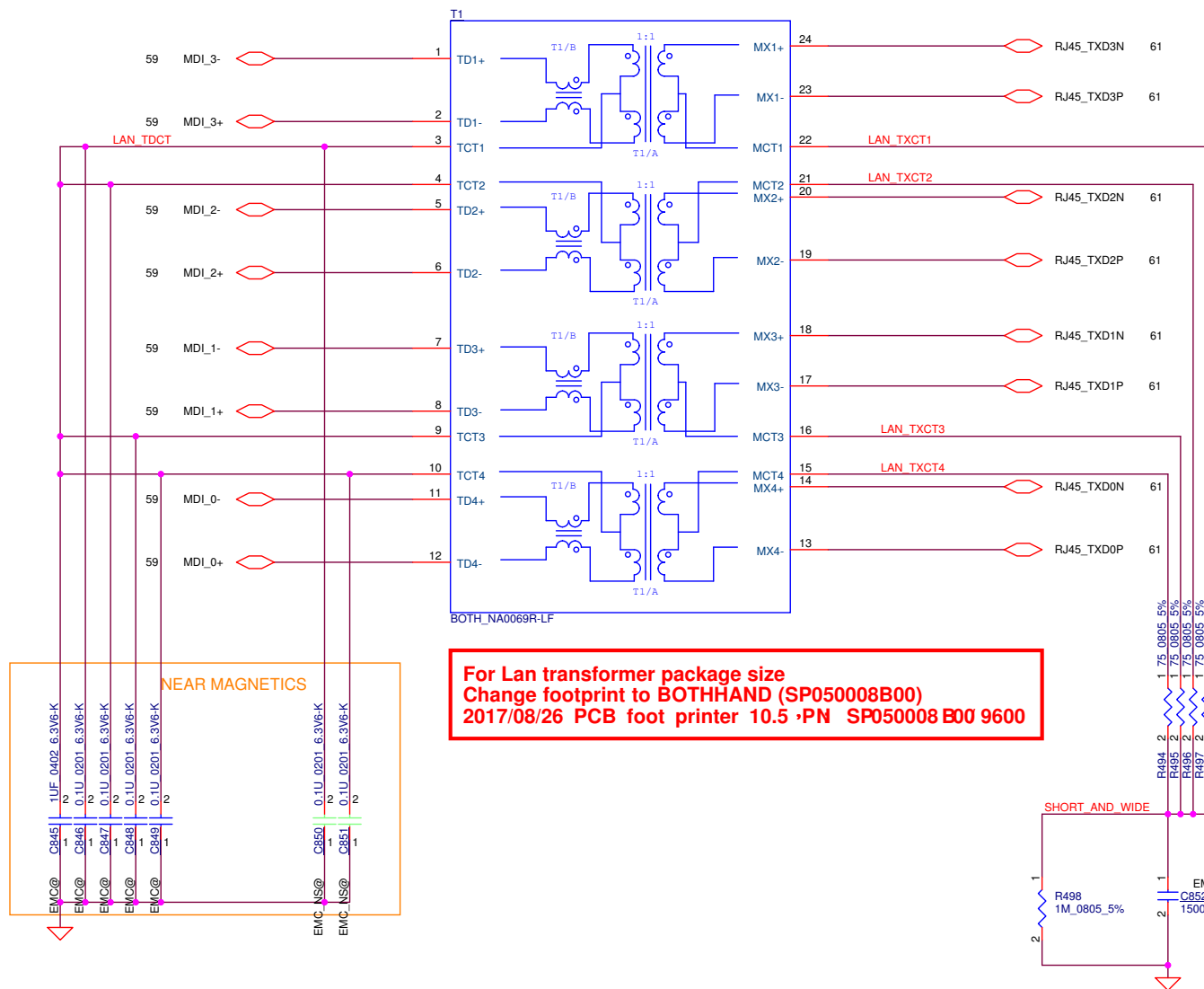
SIM	Name	Pin	Description	SIM contact ^a	Notes
Primary	UIM1_RESET	30	Reset	2	Active low SIM reset
	UIM1_CLK	32	Serial clock	3	Serial clock for SIM data
	UIM1_DATA	34	Data I/O	7	Bi-directional SIM data line
	UIM1_PWR	36	SIM voltage	1	Power supply for SIM
	SIM_DETECT	66	SIM indication	-	Input from host indicating whether SIM is present or not <ul style="list-style-type: none"> • Grounded if no SIM is present • No-connect (floating) if SIM is inserted
	UIM_GND		Ground	5	Ground reference UIM_GND is common to module ground

LAN

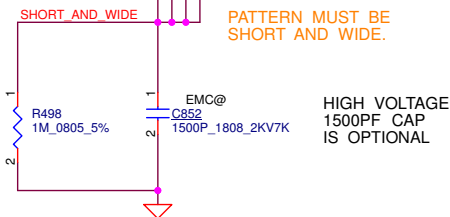


Vinafix.com

LAN



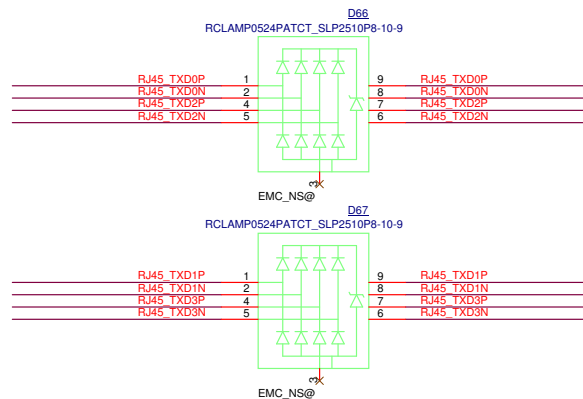
For Lan transformer package size
Change footprint to BOTHHAND (SP050008B00)
2017/08/26 PCB foot printer 10.5 ·PN SP050008 B00 9600



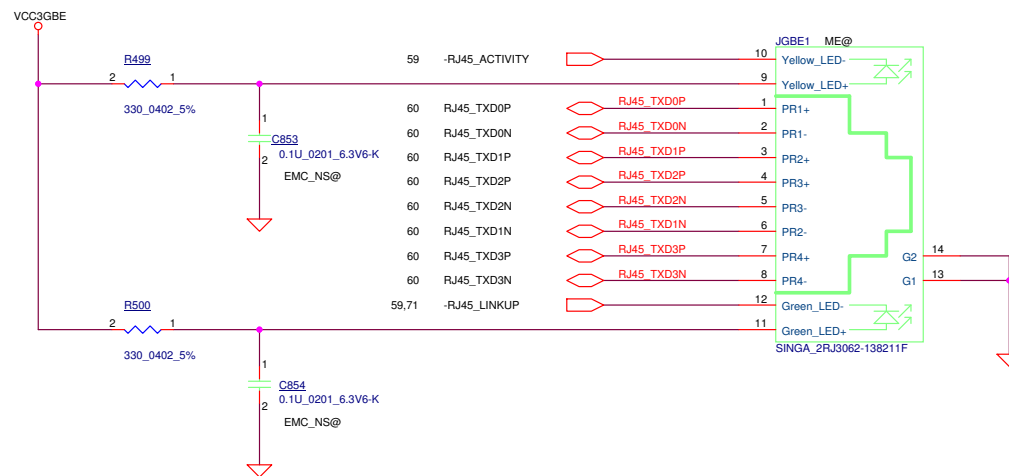
LANT1

Vendor	P/N
TAIMAG	SP050007V0J IH-189-A LAN
Bothhand	SP050008B00 NA69LF

LAN

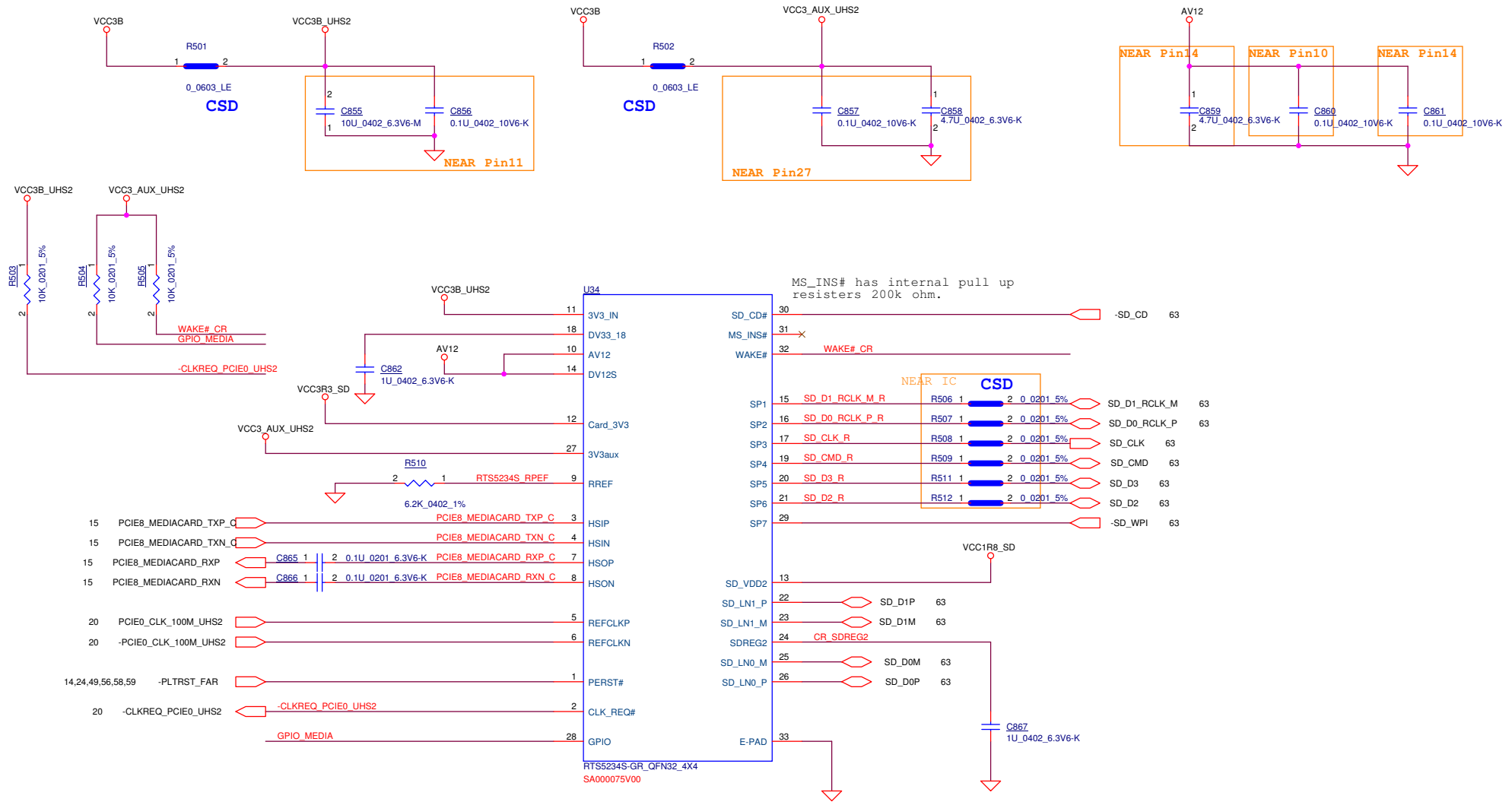


D23,D24	1st:Semtech RCLAMP0524PATCT (SC300000T0J)
	2nd:LittelFuse SP3012-04UTG-1 MO-229 (SC300003900)
	3th:LittelFuse SP3012-04UTG UDFN (SC300003800)



LC Future Center Secret Data		Project Name	
LCFC		Walter-3	
Rev	Title	GBE_RJ45 CONNECTOR	
0.5			
Date: Monday, June 25, 2018		Sheet	61 of 117

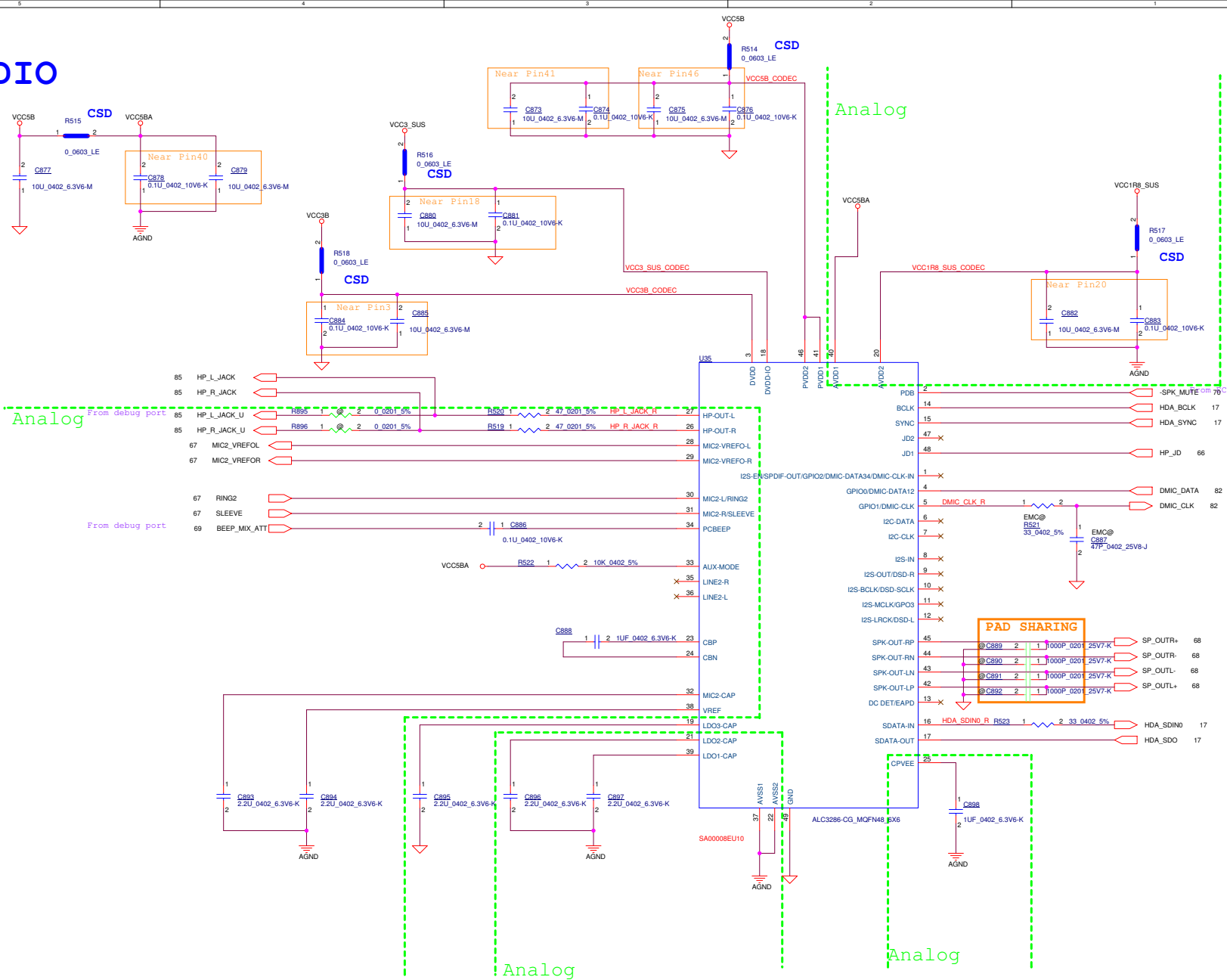
Card Reader



Card Reader

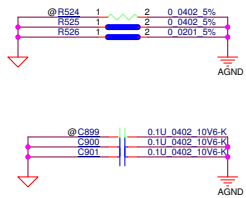
Normal type	UHS-II SD Slot	UHS II Mode
Pin No	SD Mode	
1	CD/DAT3	
2	CMD	
3	VSS1	
4	VDD1	
5	CLK	VDD1
6	VSS2	
7	DAT0	RCLKP
8	DAT1	RCLKM
9	DAT2	
10		VSS3
11		D0P
12		D0M
13		VSS4
14		VDD2
15		D1M
16		D1P
17		VSS5
18		
19		
20		
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AUDIO



Changr source to ALC3286-VA2-CG (SA00008EU10)

2017/08/28



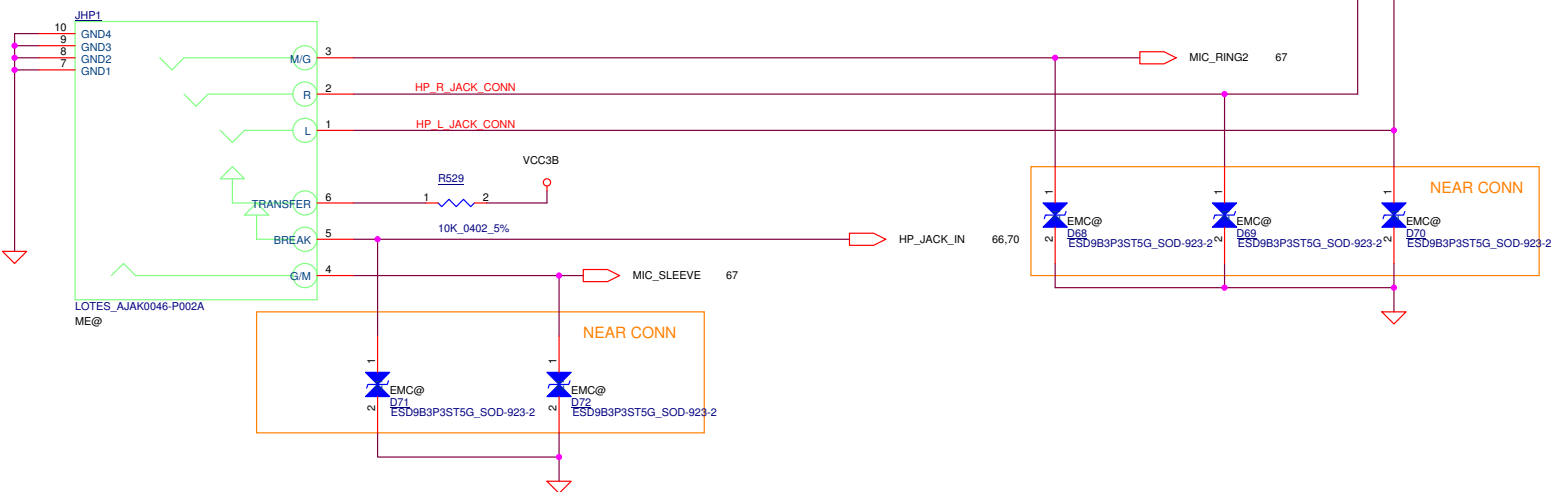
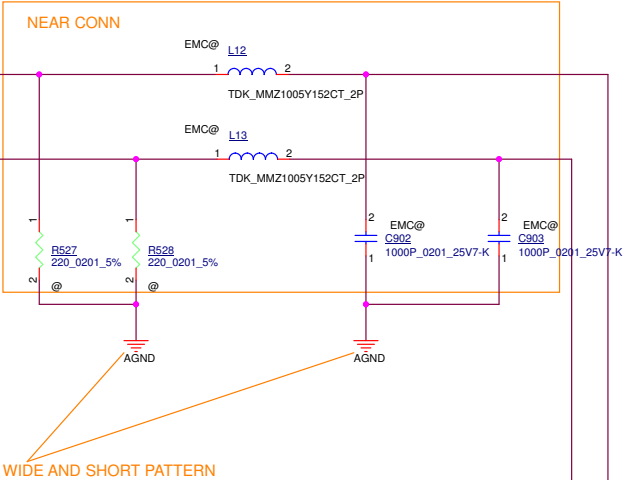
AUDIO

From debug port

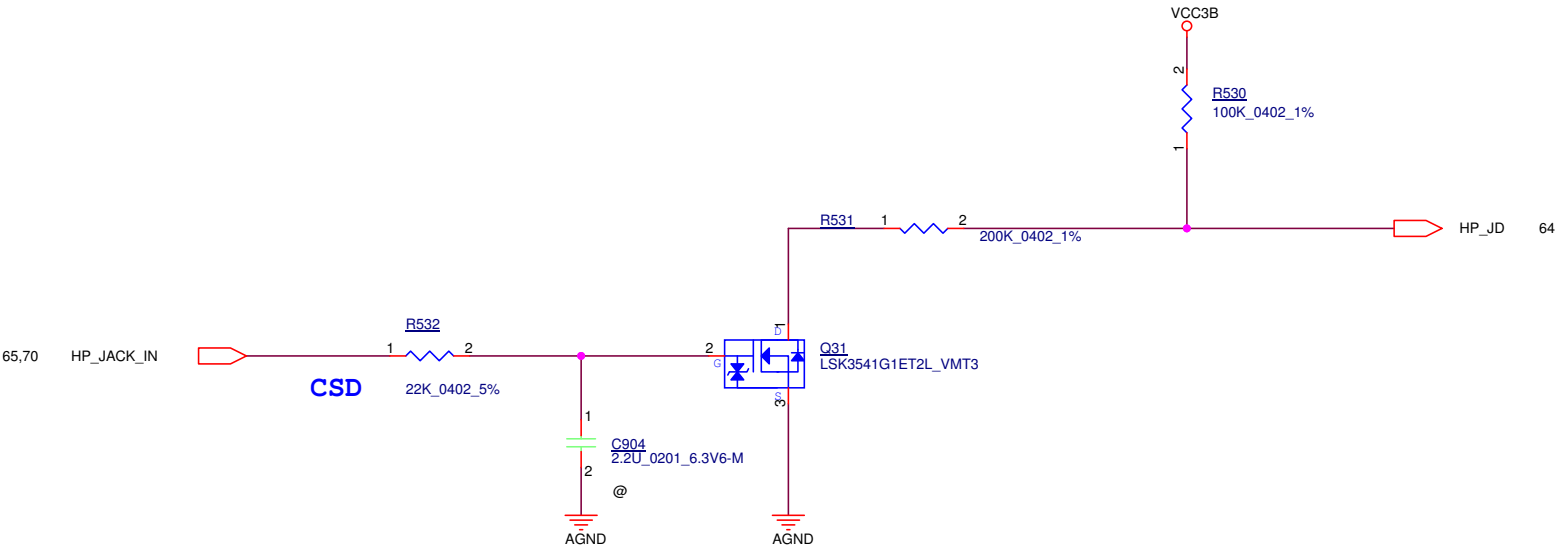
85 HP_L_UART_RX

From debug port

85 HP_R_UART_TX

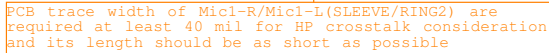


AUDIO

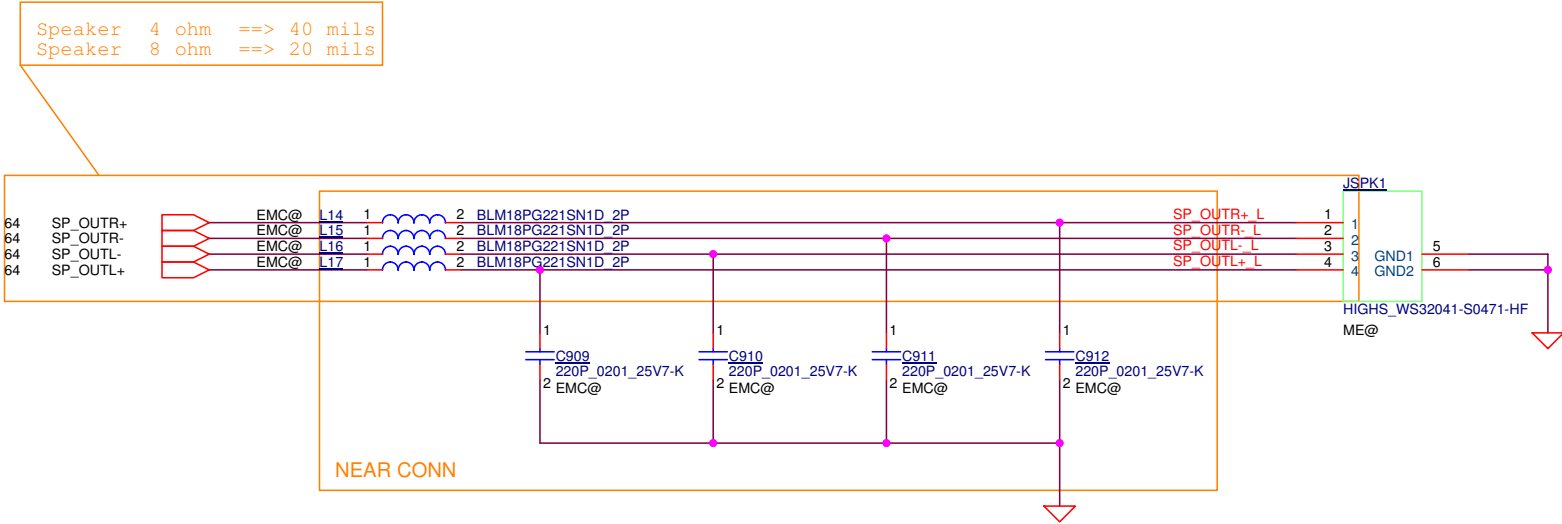


LC Future Center Secret Data		Project Name	
		Walter-3	
		Rev 0.5	Title AUDIO JACK SENSE
Date: Monday, June 25, 2018		Sheet 66 of 117	

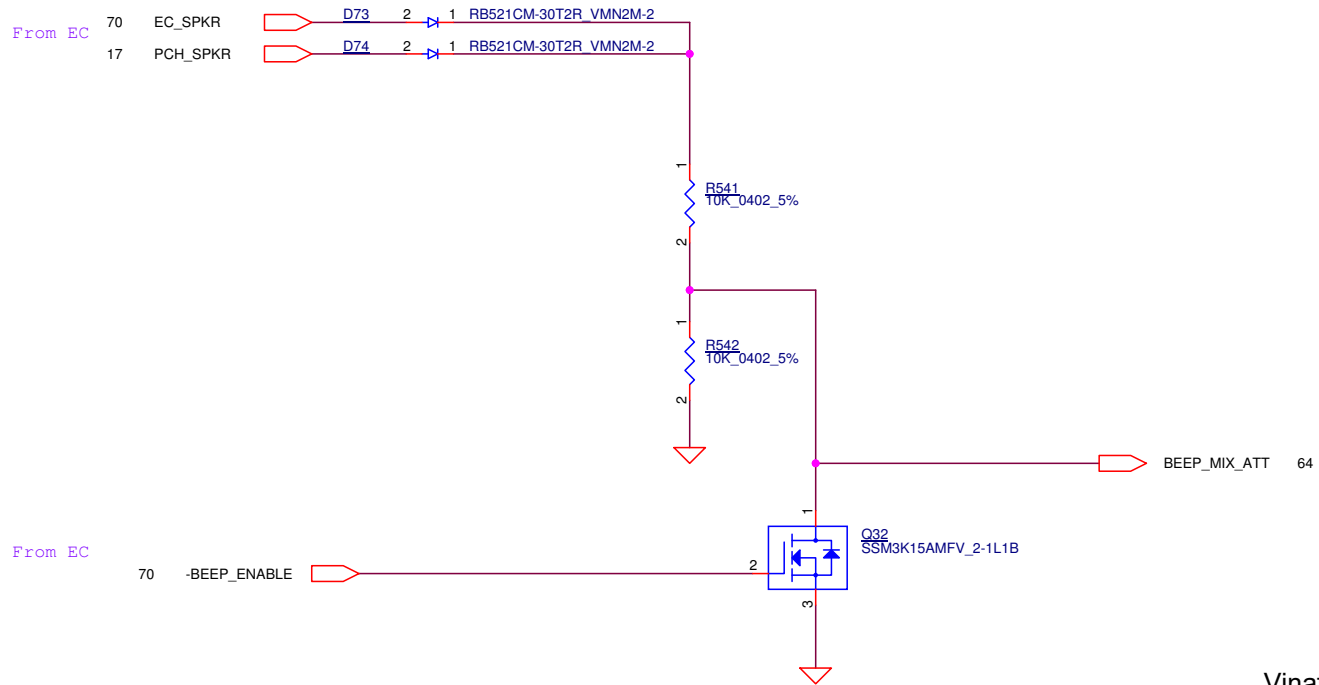
AUDIO



AUDIO



AUDIO



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LC Future Center Secret Data



Project Name

Walter-3

Rev

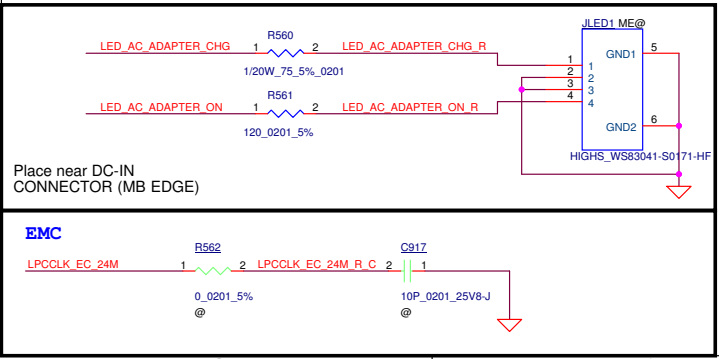
0.5


Title

AUDIO BEEP

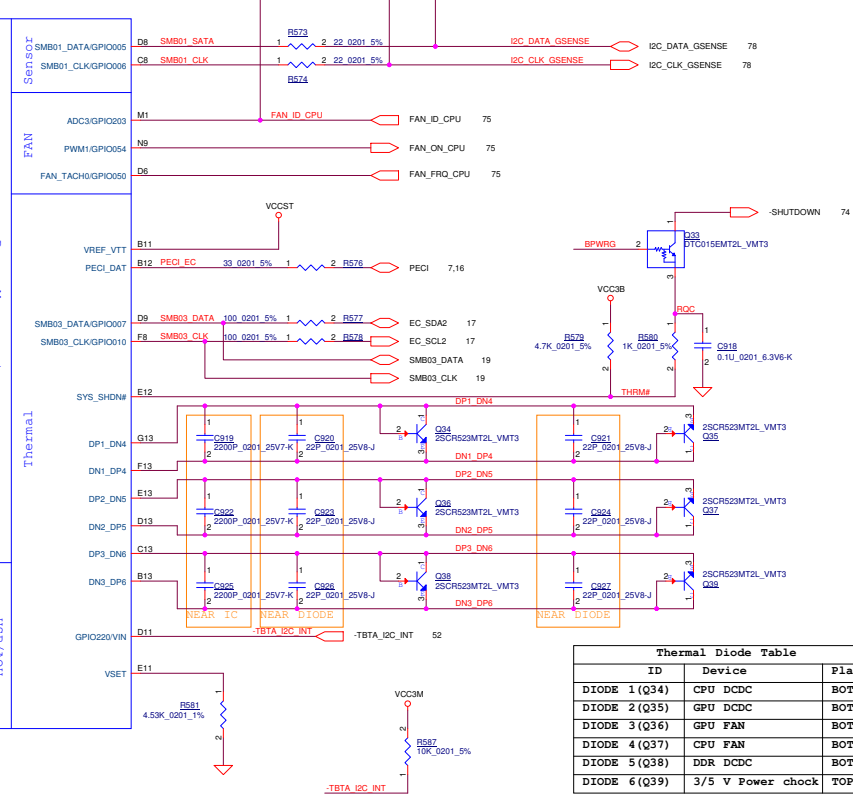
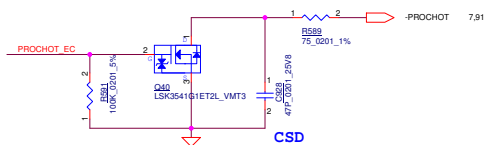
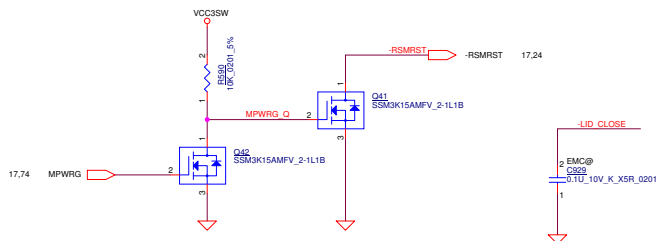
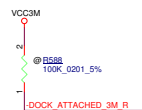
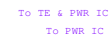
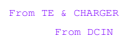
Date: Monday, June 25, 2018

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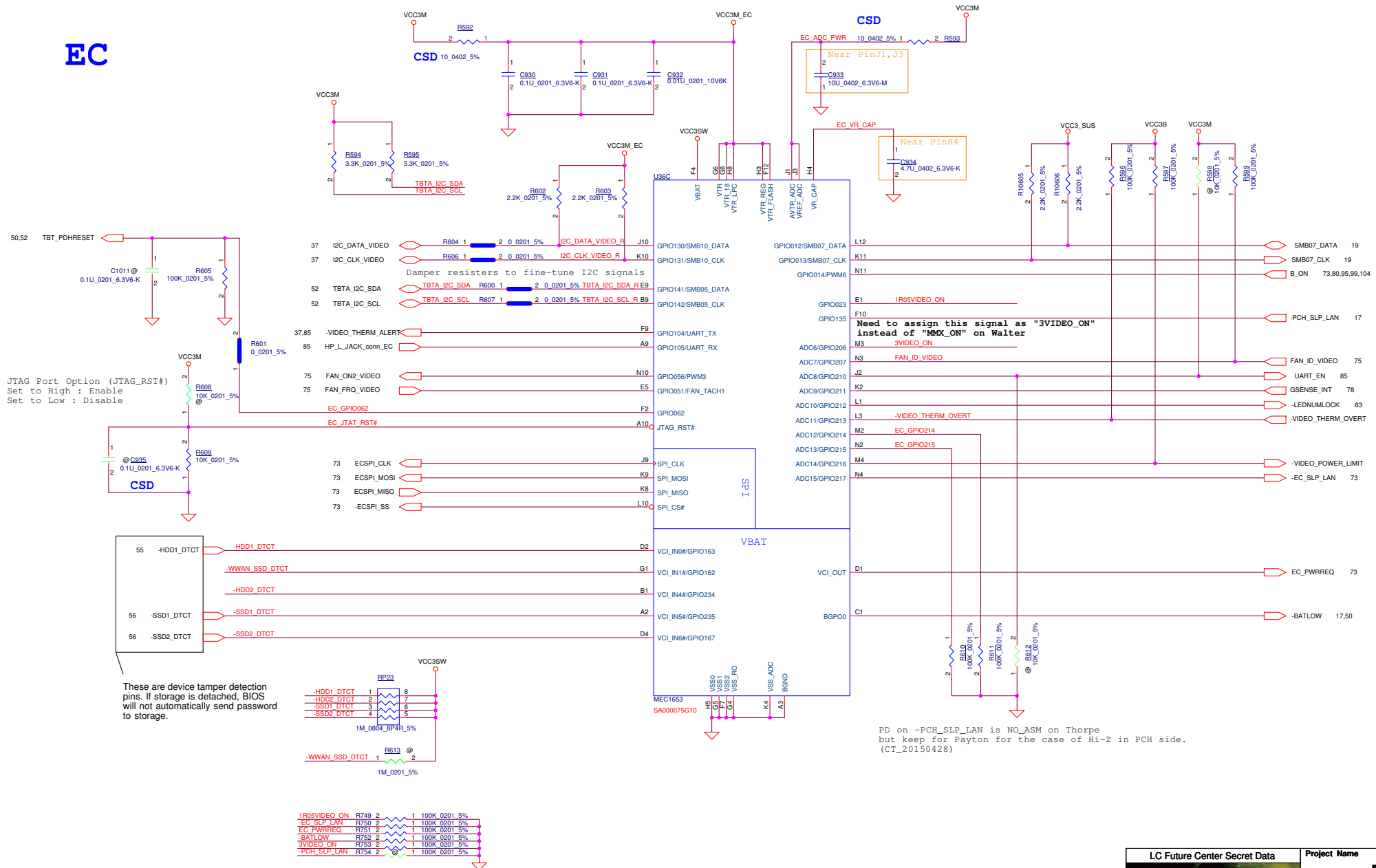
LC Future Center Secret Data		Project Name	
		<i>Walter-3</i>	
		Rev 0.5	Title MEC1653L(1/3)
Date: Monday, June 25, 2018		Sheet	70 of 117

EC



Thermal Device Table		
ID	Device	Placed on
DIODE 1 (Q34)	CPU DCDC	BOT
DIODE 2 (Q35)	GPU DCDC	BOT
DIODE 3 (Q36)	GPU FAN	BOT
DIODE 4 (Q37)	CPU FAN	BOT
DIODE 5 (Q38)	DDR DCDC	BOT
DIODE 6 (Q39)	3/5 V Power chock	TOP

EC



THINK ENGINE

Rohm Think Engine-2 Short term solution

AND LOGIC. Once -PCH_SLP_S3 is de-asserted
VCCST_PWRGD and IMVP VR_ON should be de-asserted in <= 1 usec.
These are tCPU28 and tPLTI7 defined in Intel SKL-H PDG.
(CT_20141216)

From EC & CHARGER

From EC/ PWR IC/Tunderbolt

EMC

ECSPi CLK R

Project Name

Walter-3

Rev

0.5

Title

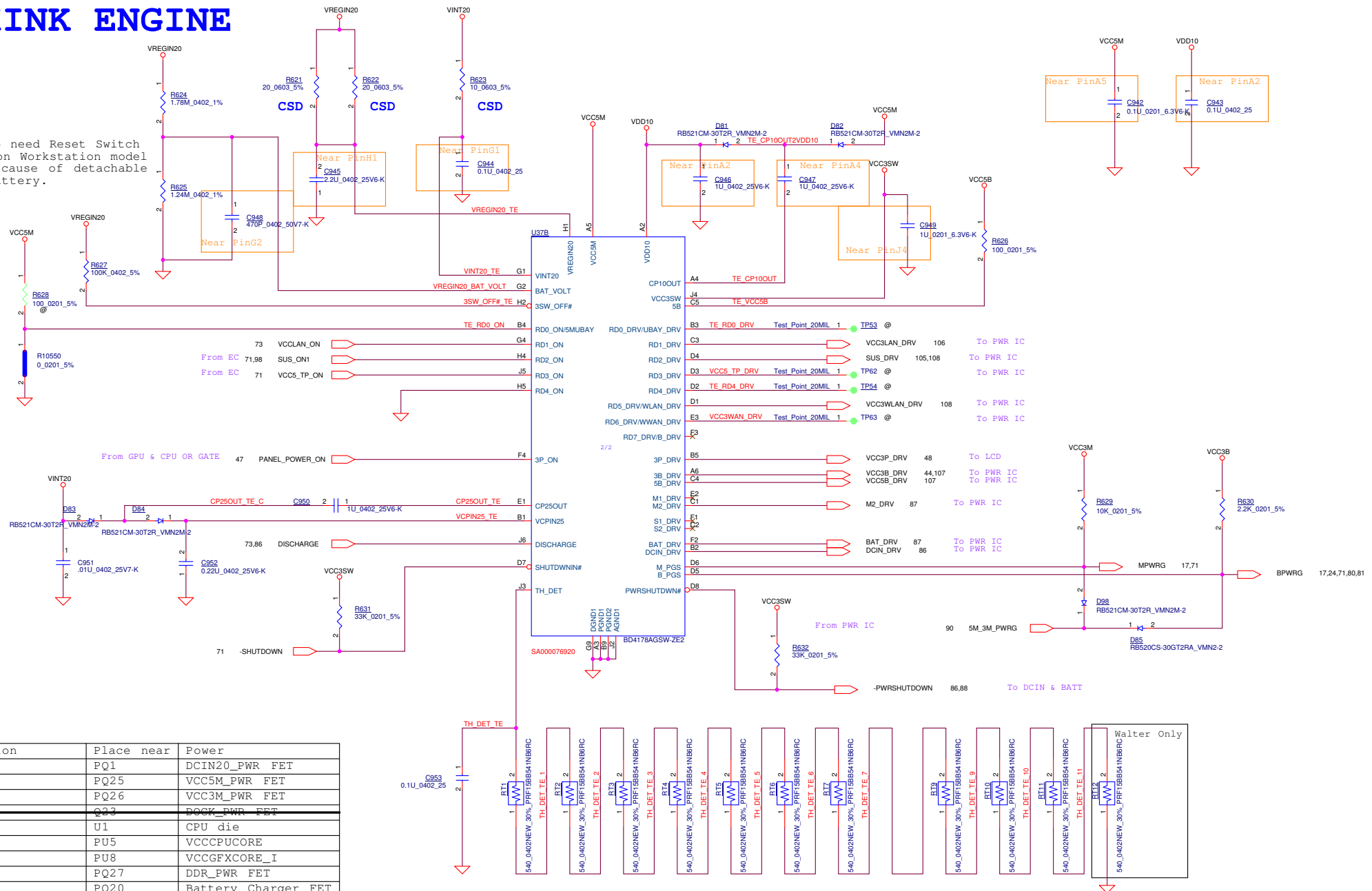
THINK ENGINE 2(1/2)

Date: Monday, June 25, 2018

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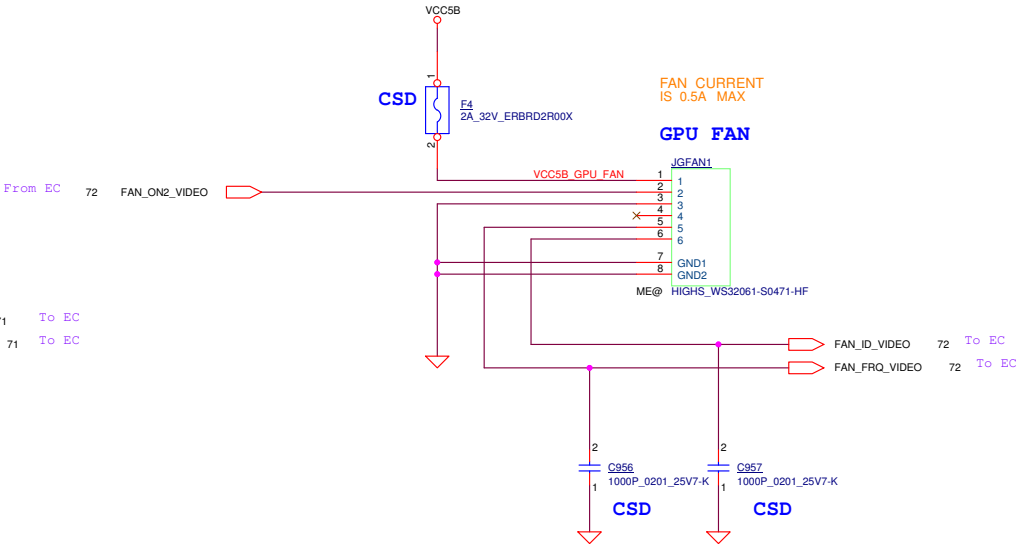
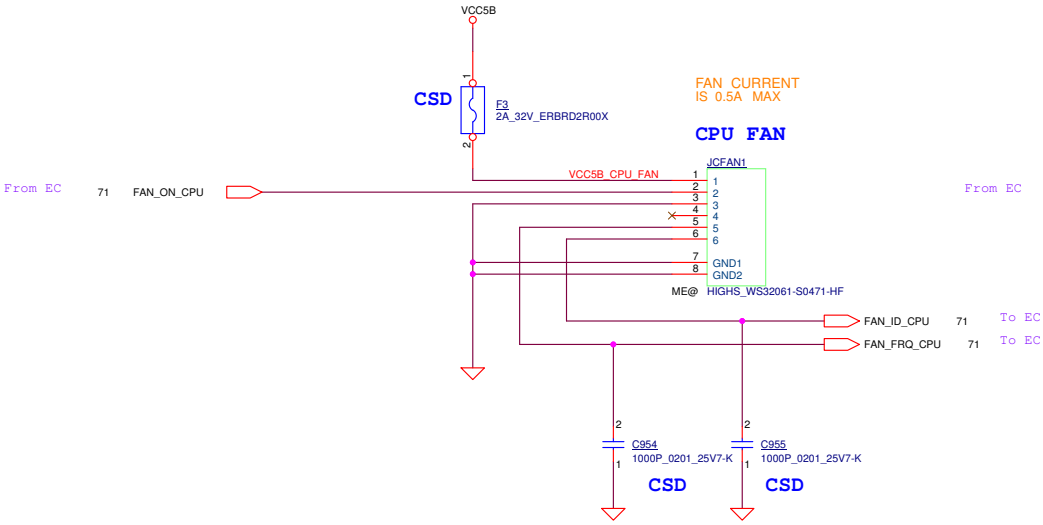
THINK ENGINE

No need Reset Switch
on Workstation model
because of detachable
battery.

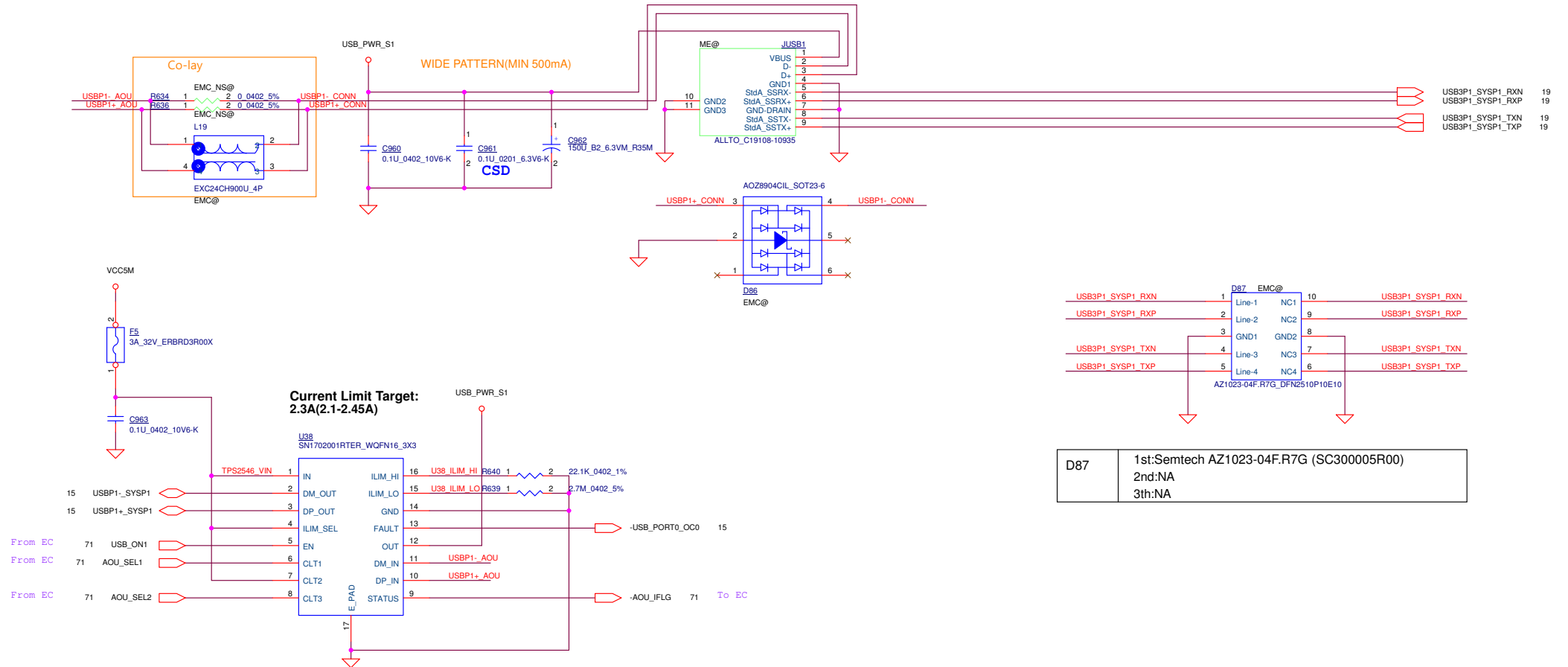


Location	Place near	Power
RT9	PQ1	DCIN20_PWR FET
RT11	PQ25	VCC5M_PWR FET
RT12	PQ26	VCC3M_PWR FET
RT8	PQ23	DOCK_PWR FET
RT6	U1	CPU die
RT7	PU5	VCCCPUCORE
RT5	PU8	VCCGFXCORE_I
RT4	PQ27	DDR_PWR FET
RT1	PQ20	Battery Charger FET
RT3	PQ46	Charge FET
RT2	PQ10	M_BAT_PWR FET
RT10	PQ100	VCCGFXCORE_D FET
PRT1(BAT_FET_HOT)	PQ11	BAT_IN


FAN



USB3.0 CONN



D87	1st:Semtech AZ1023-04F.R7G (SC300005R00)
	2nd:NA
	3th:NA

LC Future Center Secret Data		Project Name	
		<i>Walter-3</i>	
		Rev	Title
0.5	USB POWER/CONNECTOR(1/2)		
Date: Monday, June 25, 2018		Sheet 76 of 117	

USB3.0 CONN

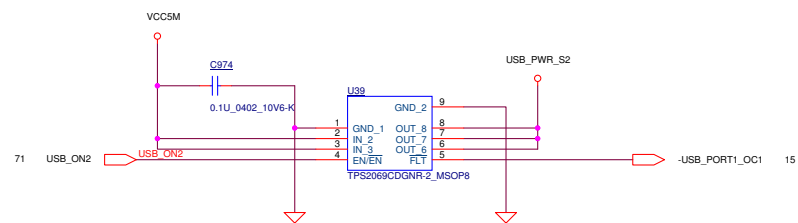
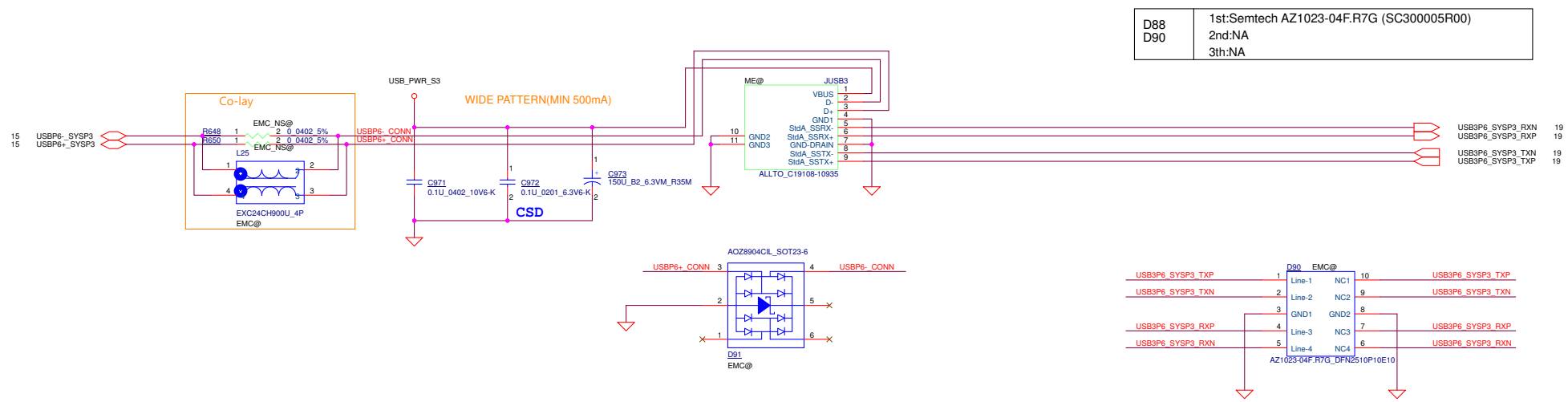
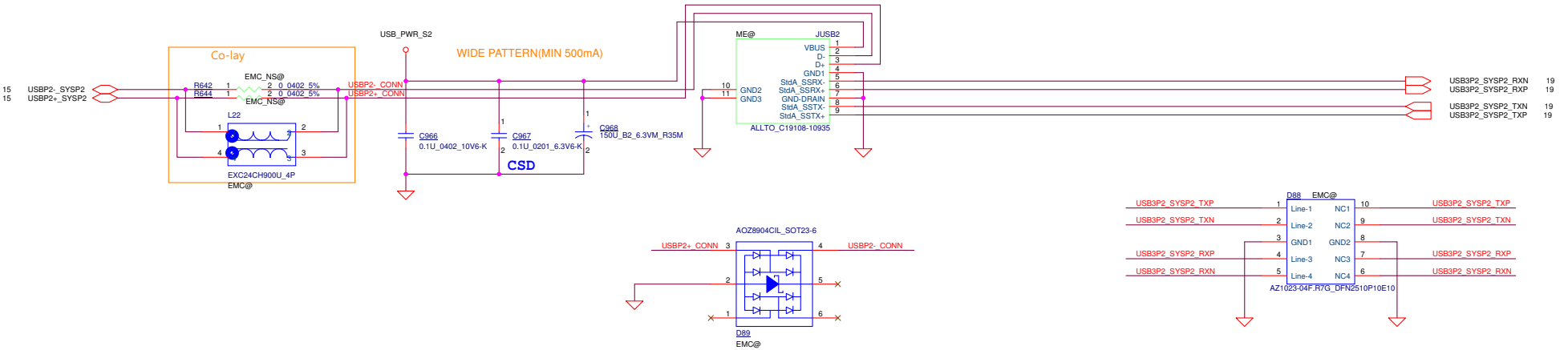


TABLE of USB3.0 Single		LCFC P/N
TI	TPS2069CDGNR-2	SA000079Y00
TI	TPS2069CDGNR	SA00005TE00

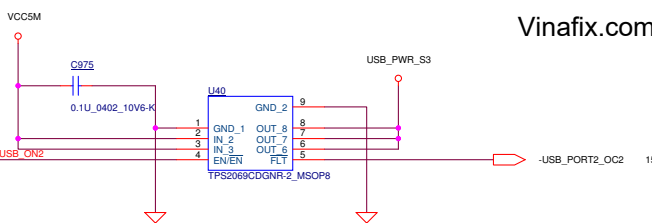


TABLE of USB3.0 Single		LCFC P/N
TI	TPS2069CDGNR-2	SA000079Y00
TI	TPS2069CDGNR	SA00005TE00

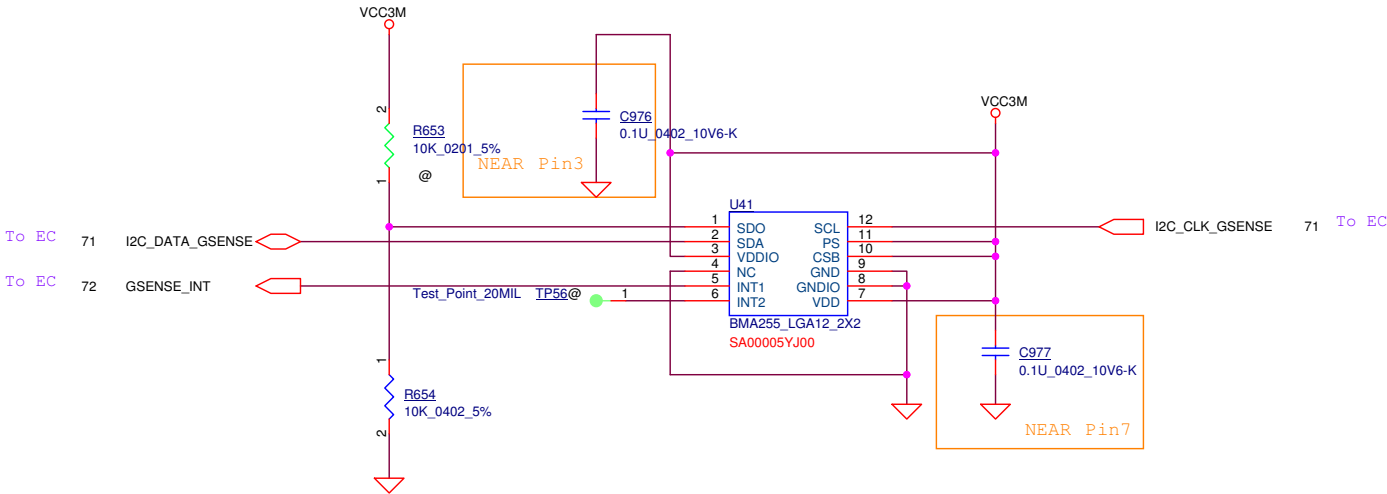
Vinafix.com

G-SENSOR


TABLE

P/N	ADDR_SEL	Address
BMA255	H	30h (W) & 31h (R)
	L	32h (W) & 33h (R)
KX022-1020	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)

TABLE of G-Sensor (GSU1)		
Vendor	P/N	LCFC P/N
BOSCH	BMA255	SA00005YJ00
Kionix	KX022-1020	SA000081E00



LC Future Center Secret Data



Project Name

Walter-3

Rev

0.5

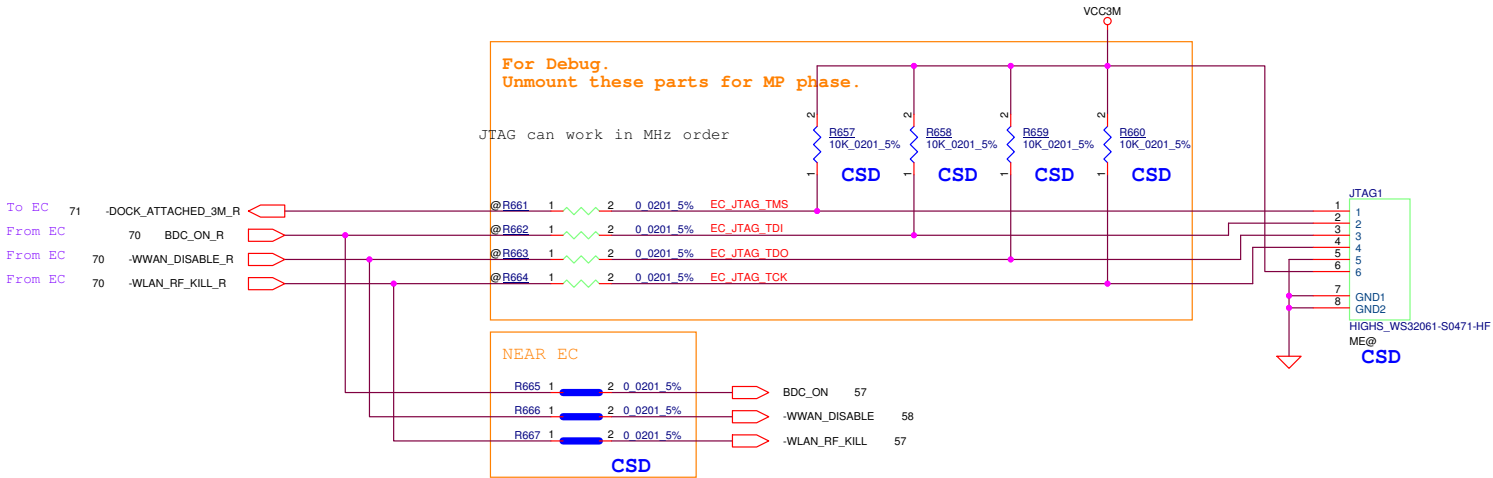
Title

APS G-SENSOR

Date: Monday, June 25, 2018

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LPC DEBUG PORT



SMBUS SWITCH

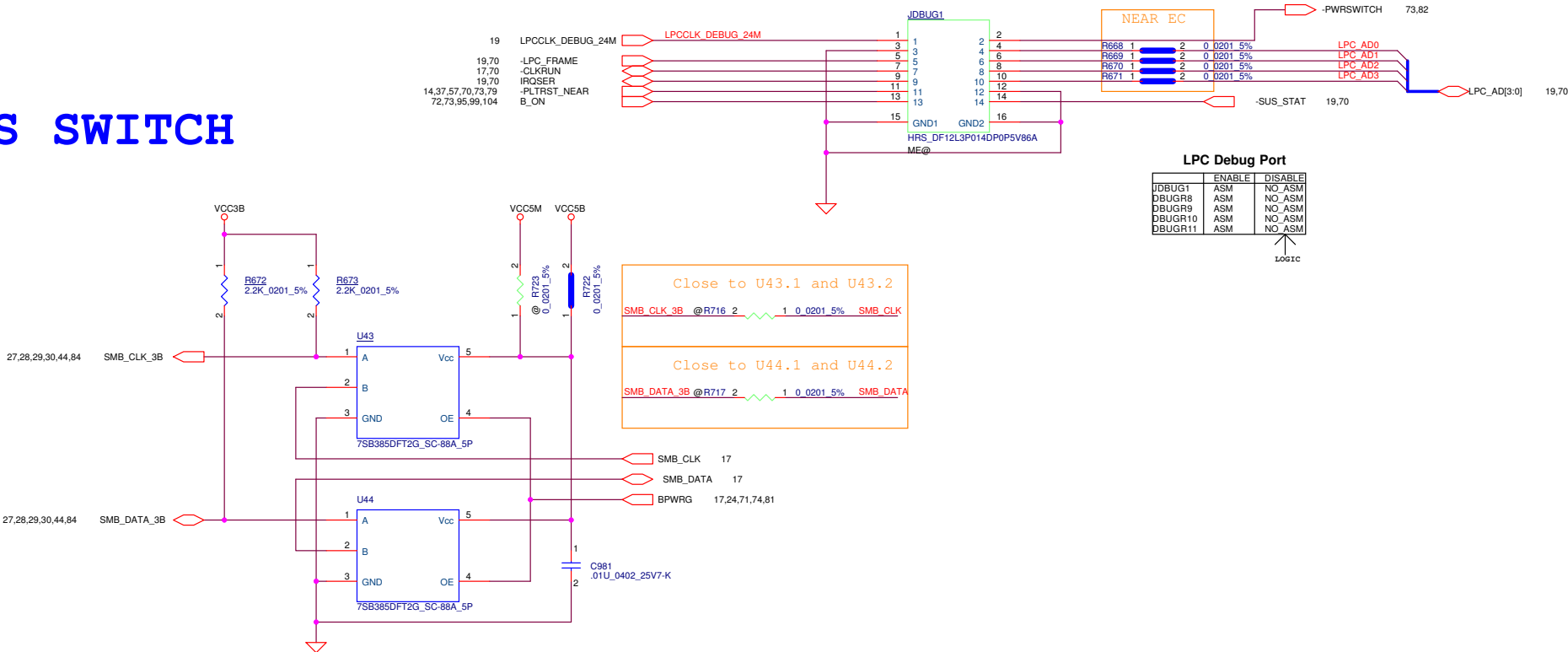
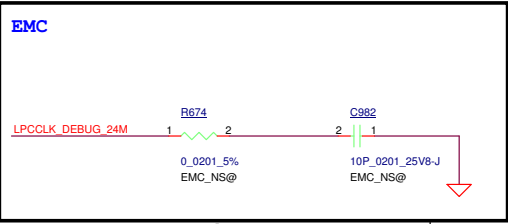


TABLE of U43/U44		
Vendor	P/N	LCFC P/N
TOCHIDA	7SB385DFT2G	SA00007CW00
ON	7SB385DFT2G	SA00007CW00

U43, U44 Symbol : SA00005US0J



LC Future Center Secret Data

LCFC

Project Name

Walter-3

Rev

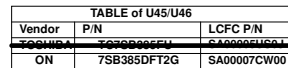
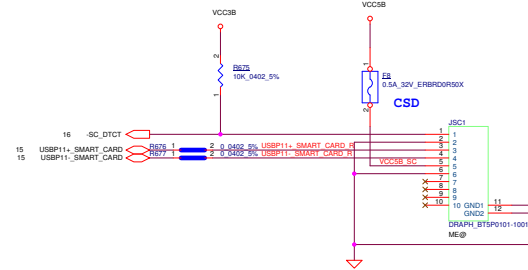
0.5

Title

SMBUS SWITCH/LPC DEBUG PORT

Date: Monday, June 25, 2018

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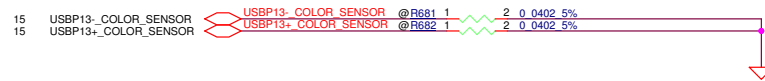


Timing diagram for PMU initialization sequence. The diagram shows the relationship between VBAT, PVDD, VEN, and PMUVCC signals. Key timing parameters include:

- t_{boot} : Boot time after PVDD is established.
- $t_{\text{VDDPAD-VEN}}$: Time between PVDD and VEN transitions.
- $t_{\text{host communication possible}}$: Time after VEN is established when host communication is possible.
- $t_{\text{VBAT(L)}}$: VBAT low pulse width.
- $t > 100 \mu\text{s}$: Minimum time between VEN and PMUVCC transitions.
- $t > 0 \text{ ms}$: Minimum time between PMUVCC and PVDD transitions.

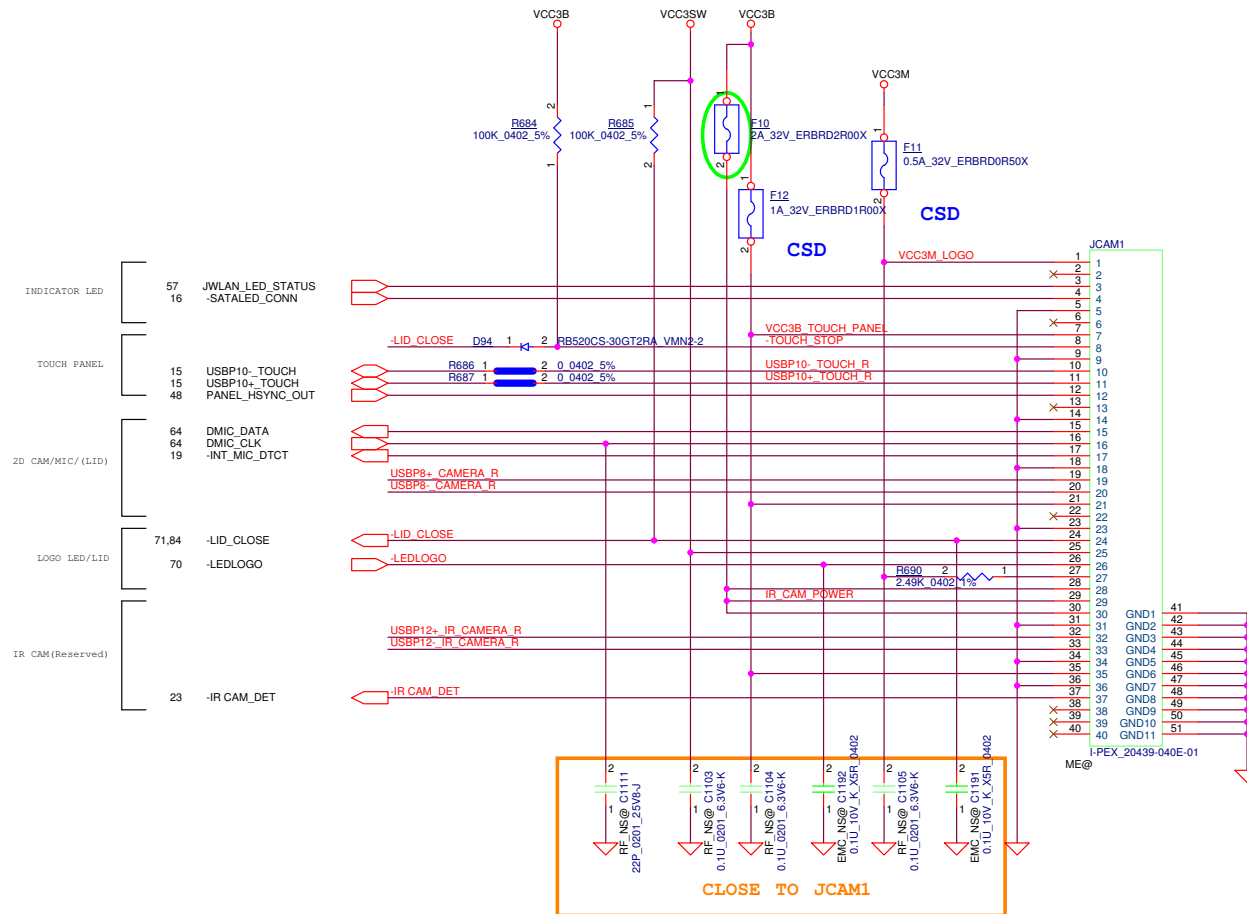
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T _{1(DWL_REQ-VE)}	Transition time from pin DWL_REQ to pin VEN	DWL_REQ, VEN voltage=HIGH	0	0.5	-	ms

COLOR SENSOR

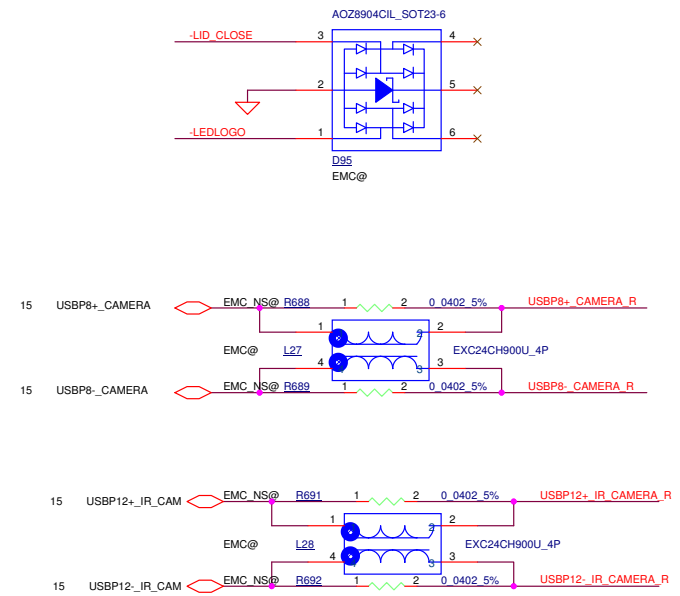
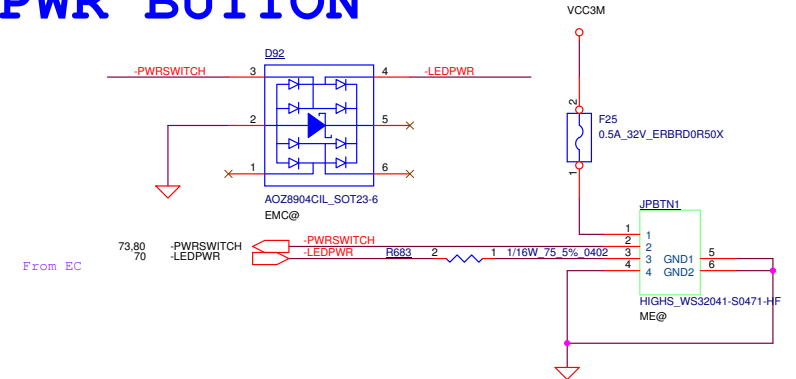


DROOP CS FUNCTION 2017/08/07

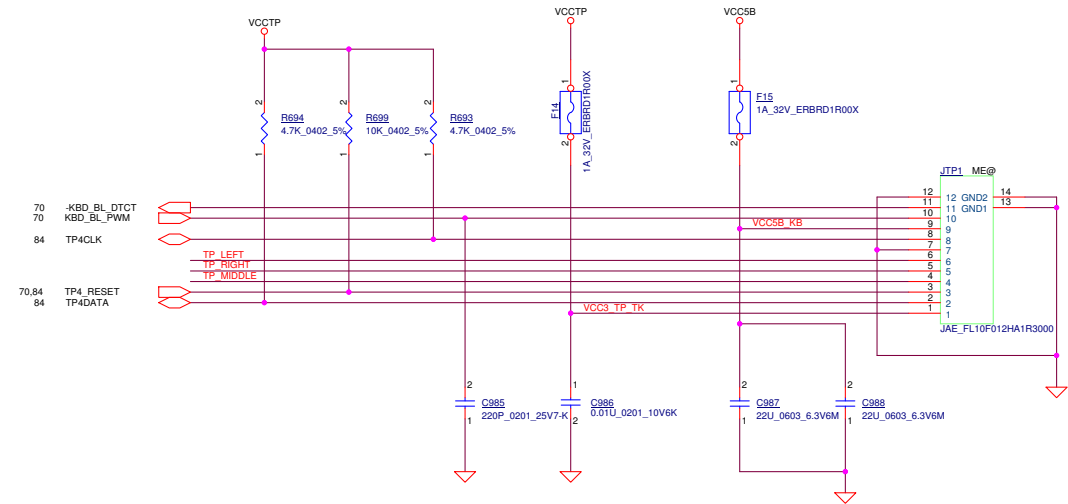
CAMERA/TOUCH



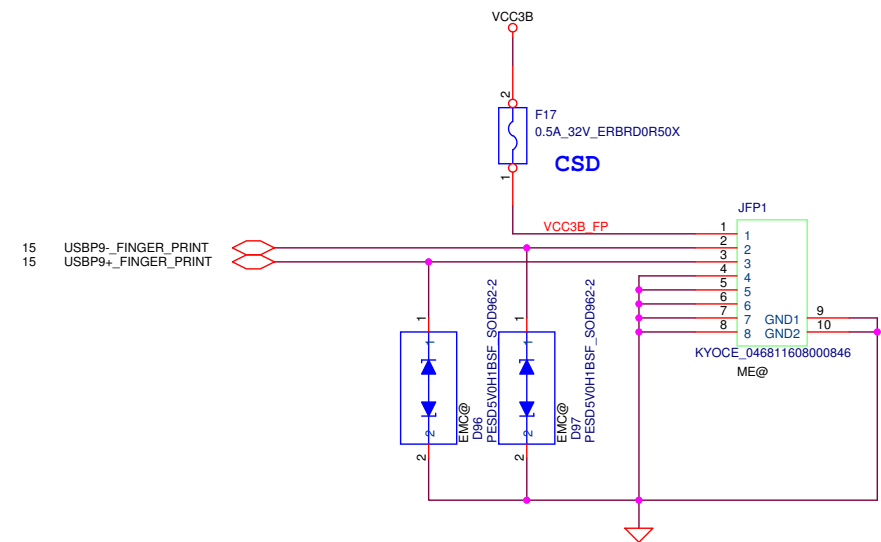
PWR BUTTON




TRACK POINT



Fingerprint



LC Future Center Secret Data		Project Name	
		<i>Walter-3</i>	
		Rev 0.5	Title CLICK PAD/FPR
		Date: Monday, June 25, 2018	
		Sheet	84 of 117

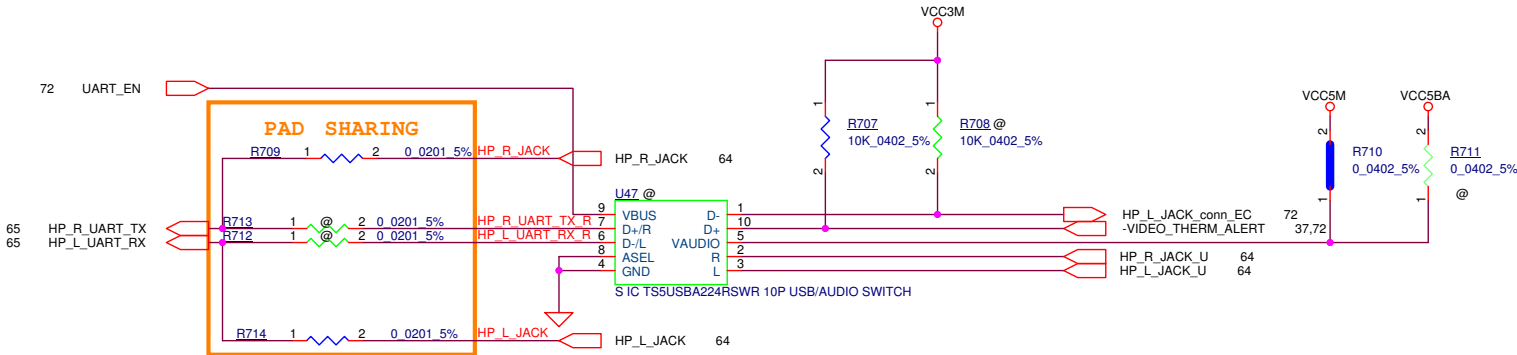
AUDIO DEBUG PORT

TABLE:

Mode	Audio	UART
UART_EN	L	H

TABLE:

Debug feature	Enable	Disable
U47	ASM	NA
R708	ASM	NA
R710	ASM	NA
R712	ASM	NA
R713	ASM	NA
R895	ASM	NA
R896	ASM	NA
R709	NA	ASM
R714	NA	ASM



DCIN

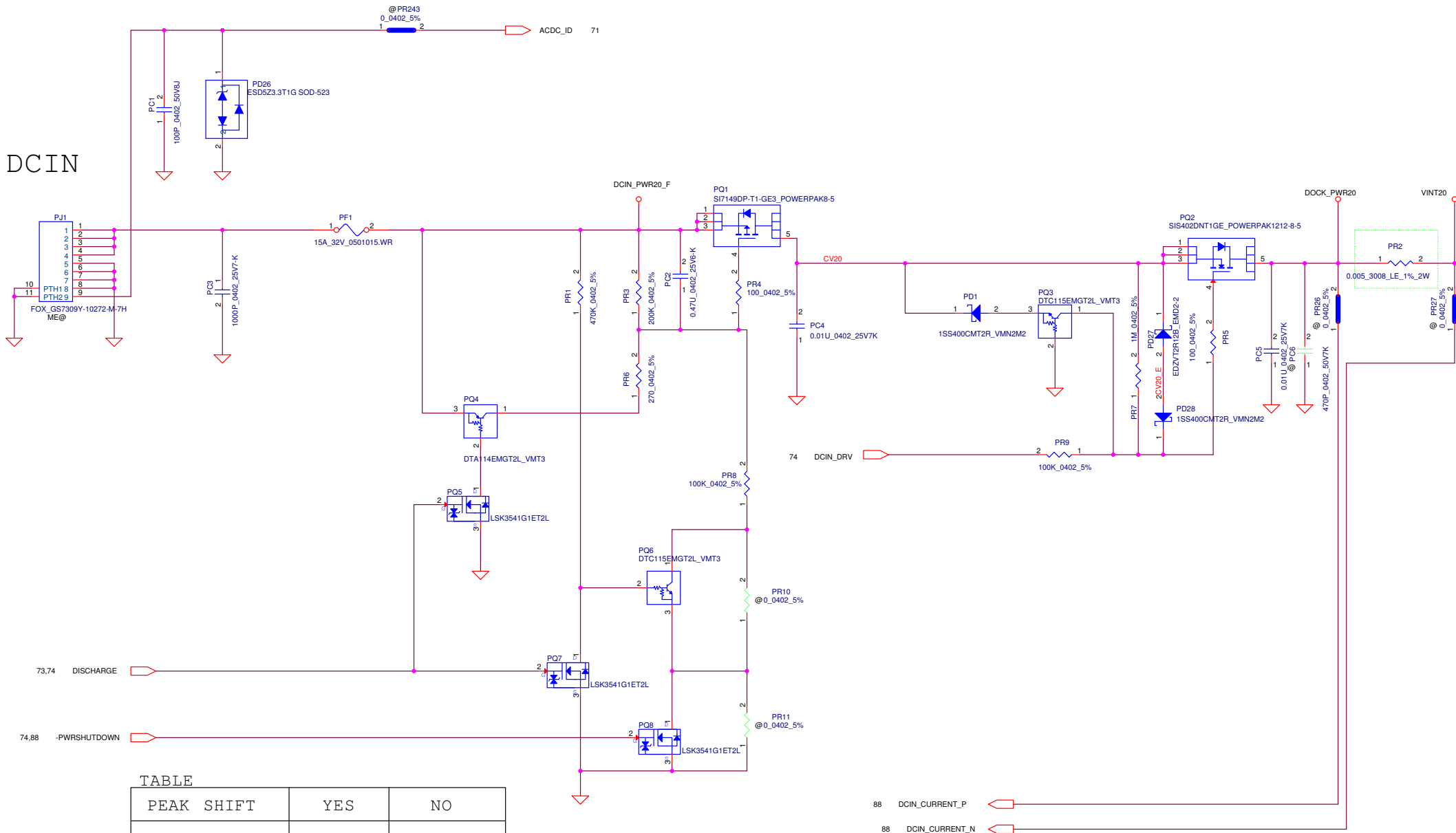
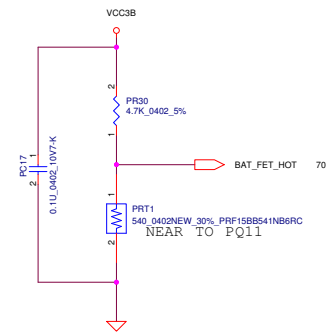
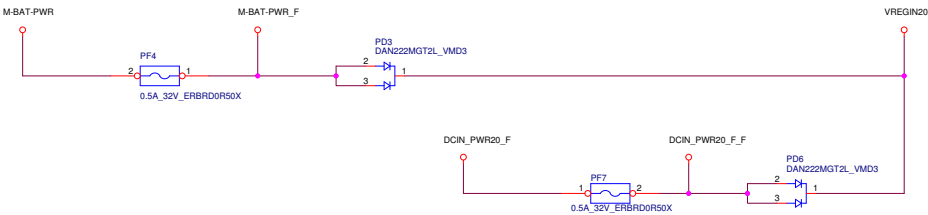
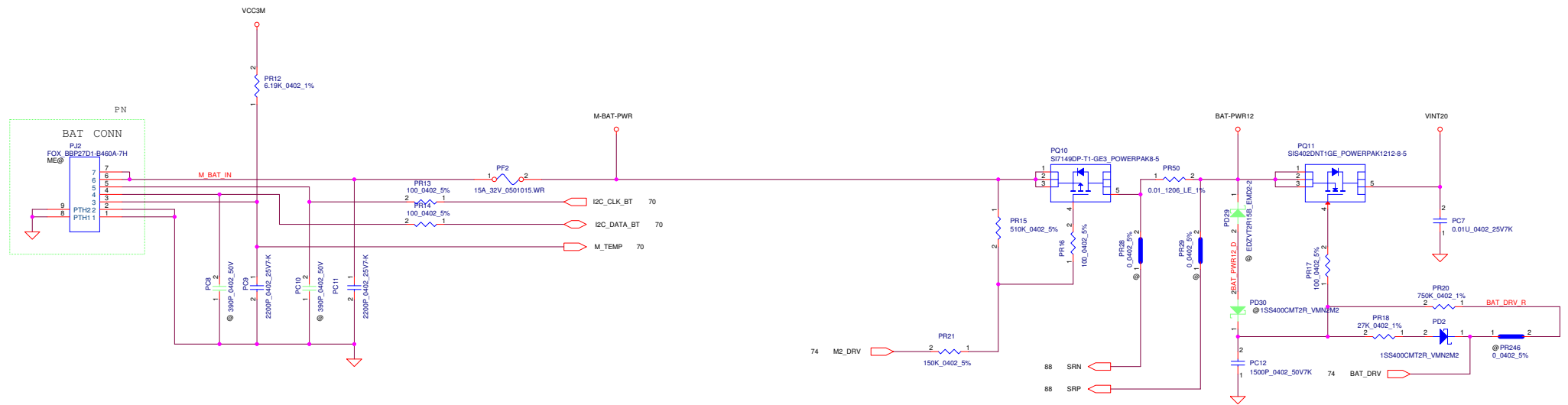
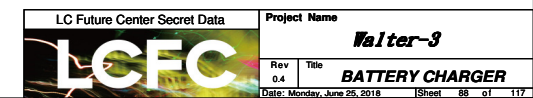


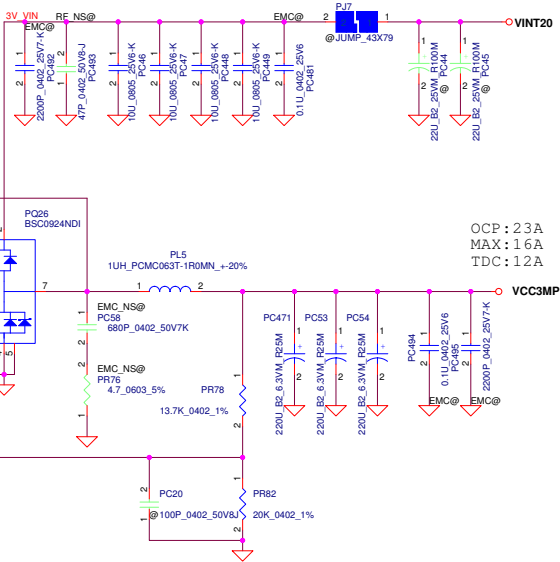
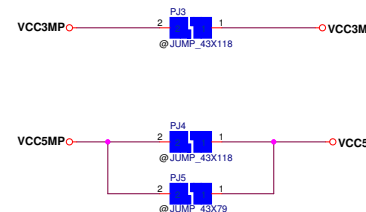
TABLE			
PEAK	SHIFT	YES	NO
	PR10	NO-ASM	ASM
	PR1	ASM	NO-ASM
	PQ6	ASM	NO-ASM
	PQ7	ASM	NO-ASM

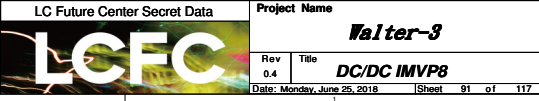
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LOGIC



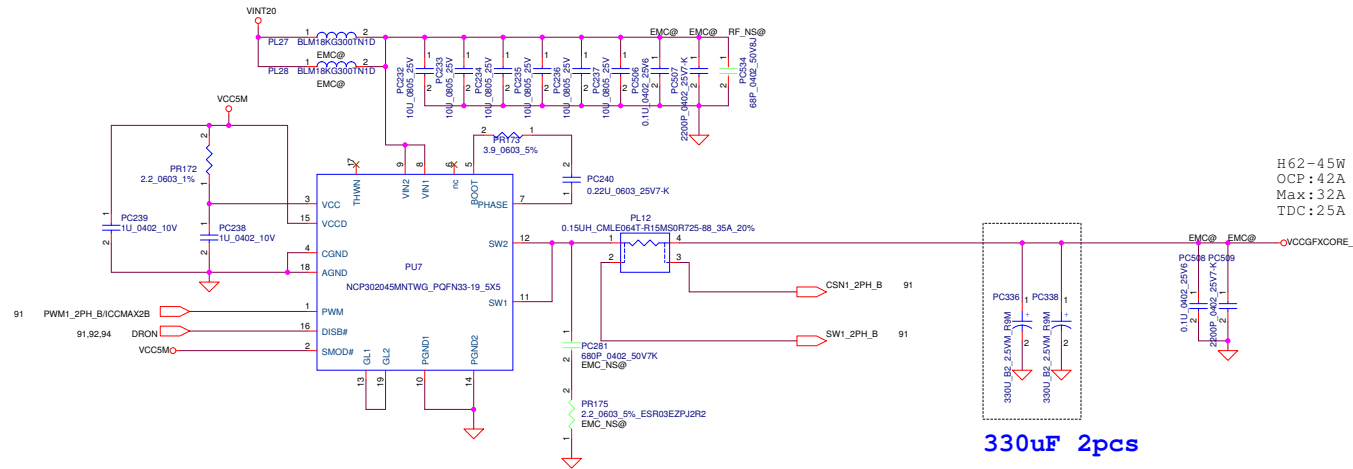


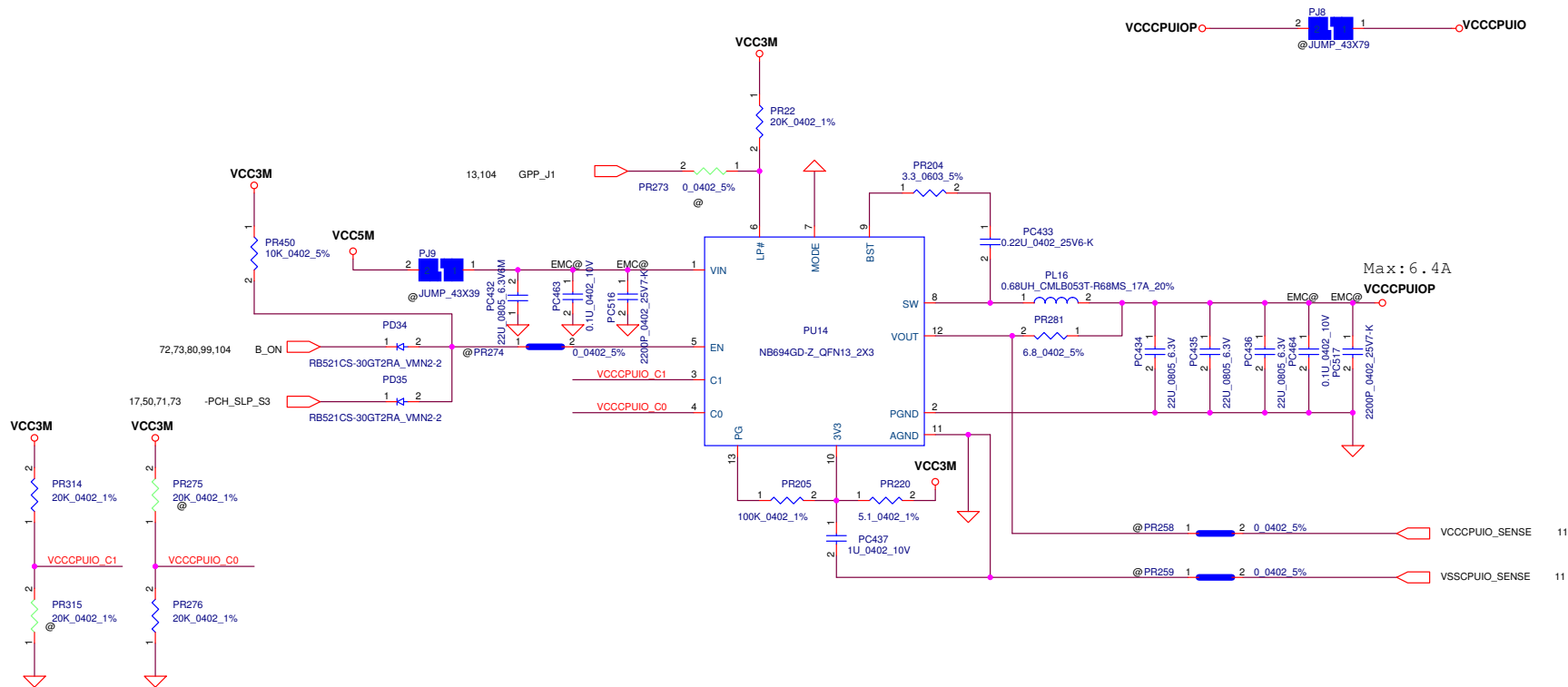
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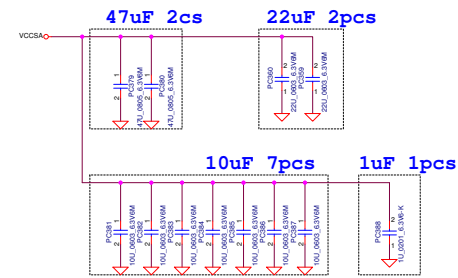
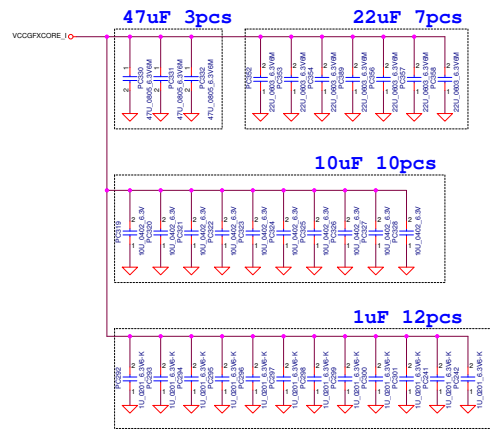
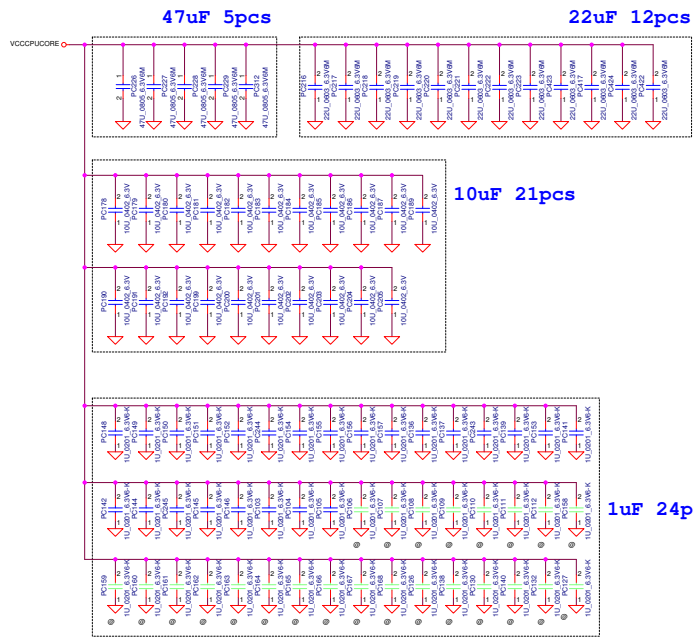
Vinafix.com



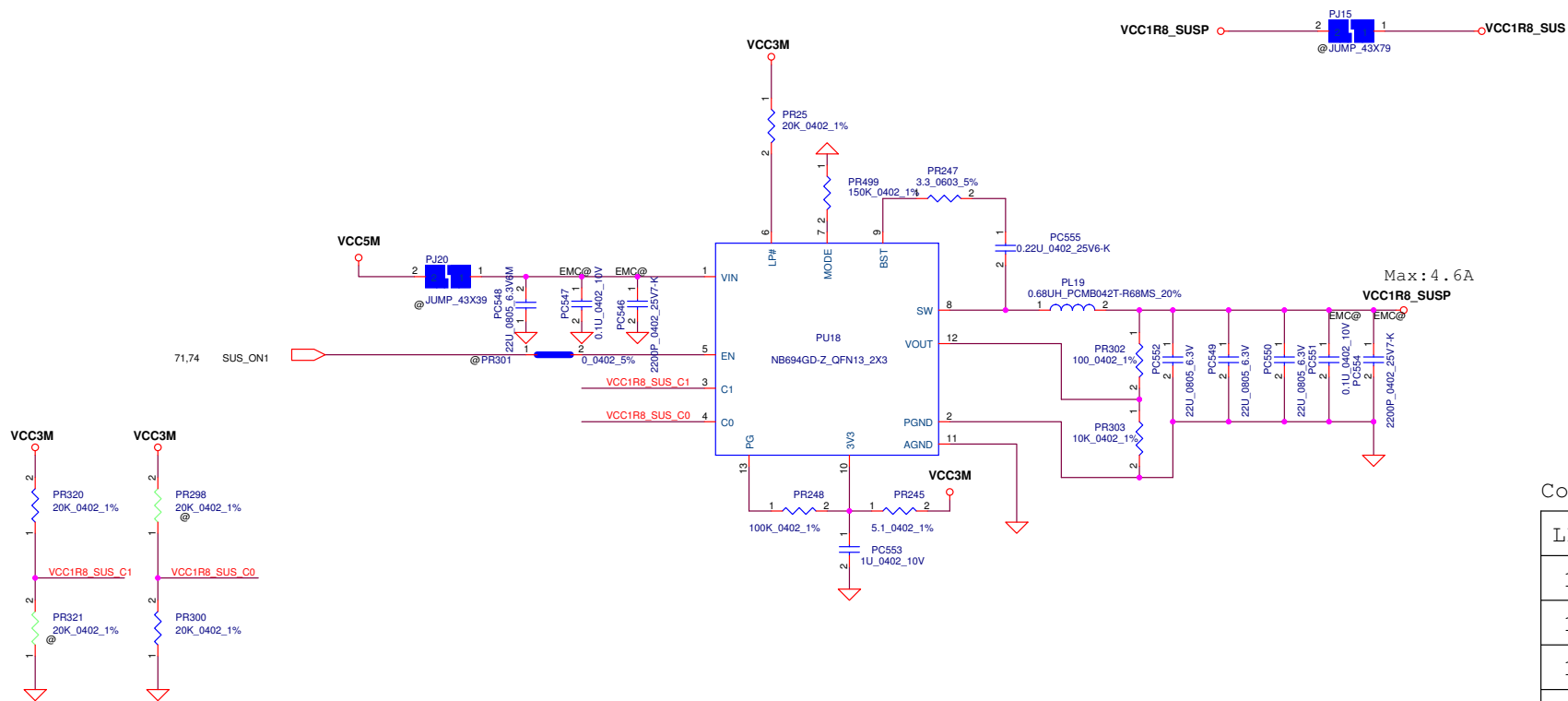


Control Bit Definitions

LP#	C1	C0	VOUT(V)
0	X	X	0
1	0	0	0.85
1	0	1	0.875
1	1	0	0.95
1	1	1	0.975

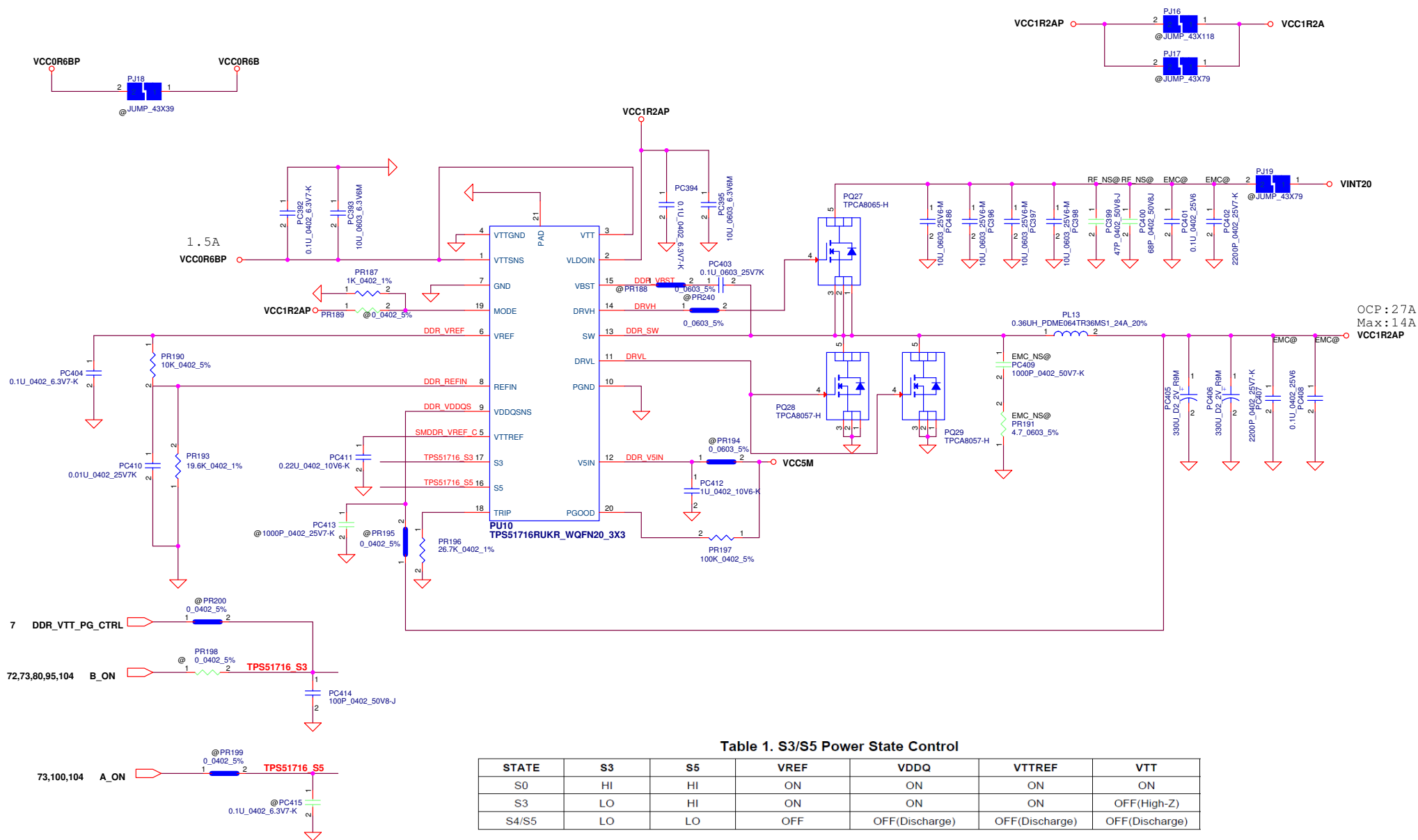


Vinafix.com



Control Bit Definitions

LP#	C1	C0	VOUT (V)
1	0	0	1.2
1	0	1	1.5
1	1	0	1.8
1	1	1	2.5



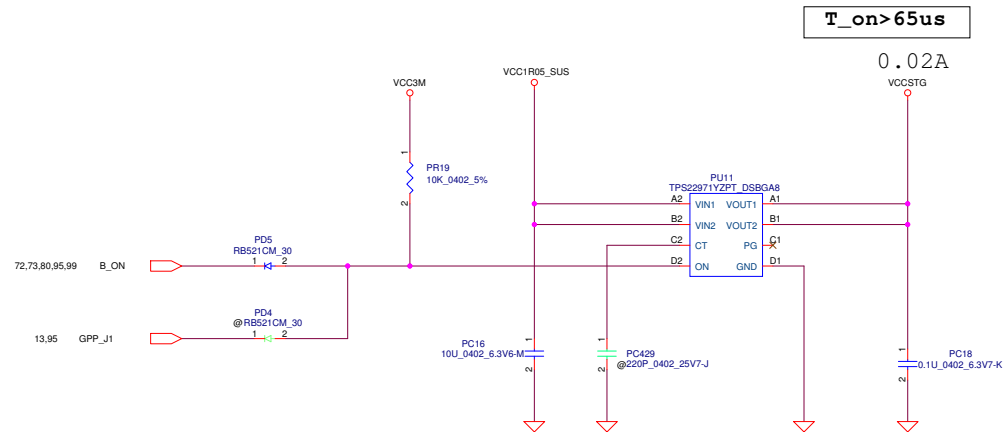
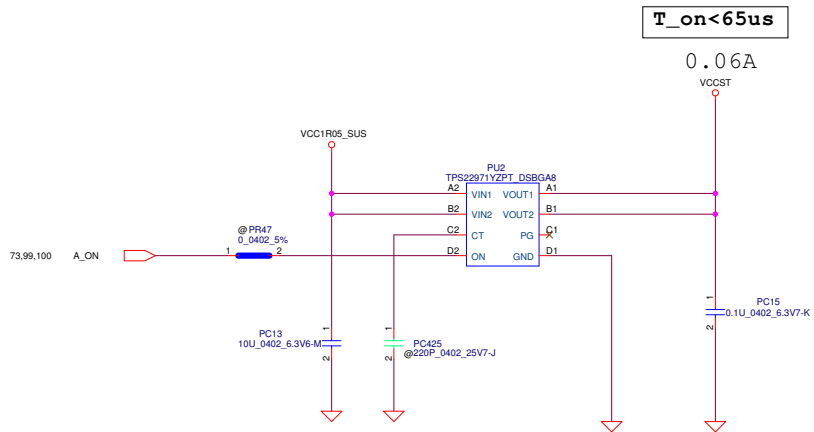
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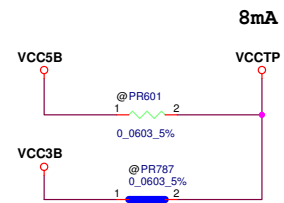
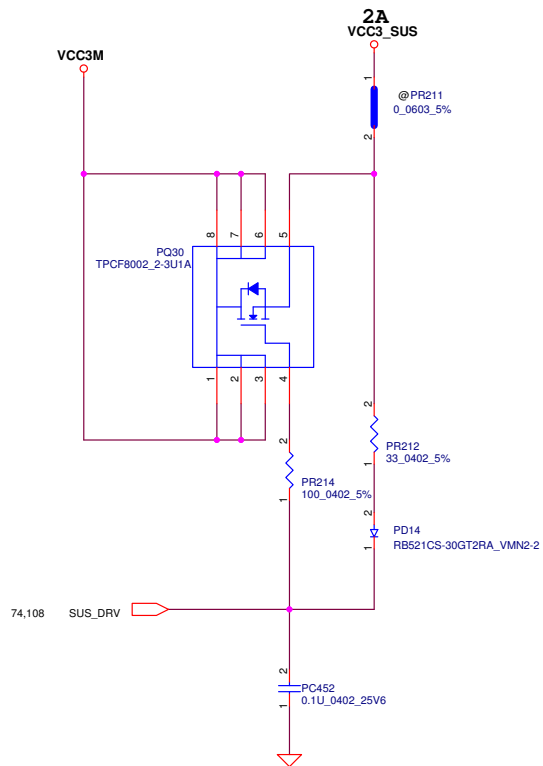
Vinafix.com

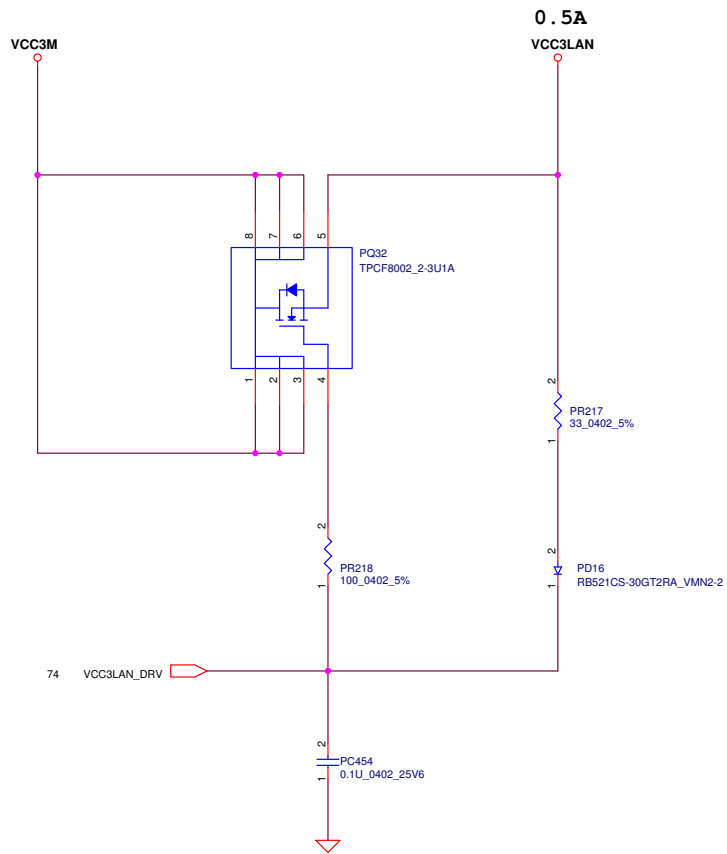
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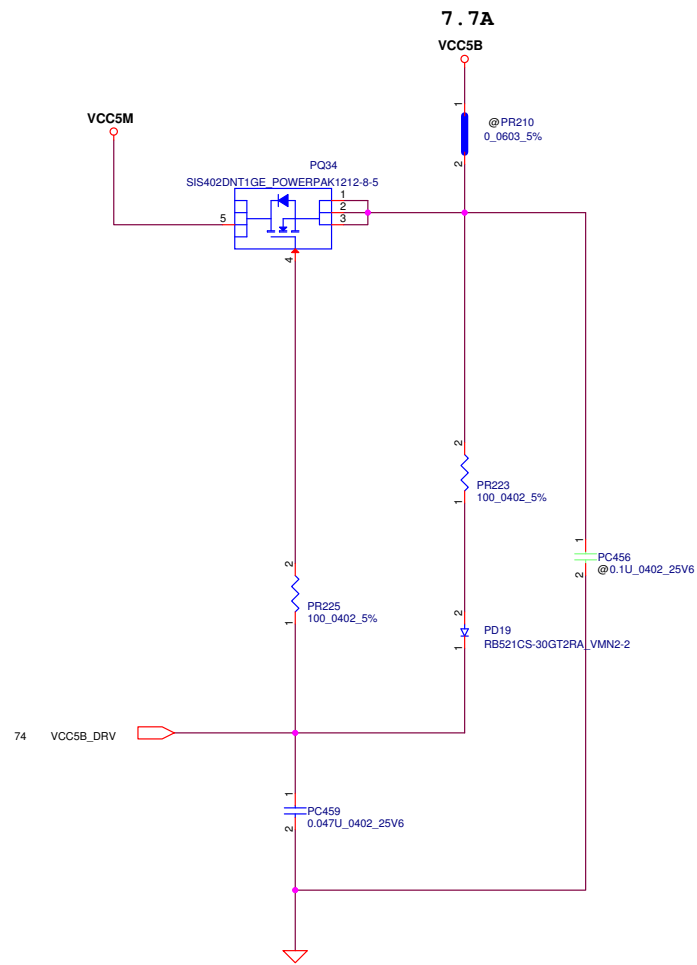
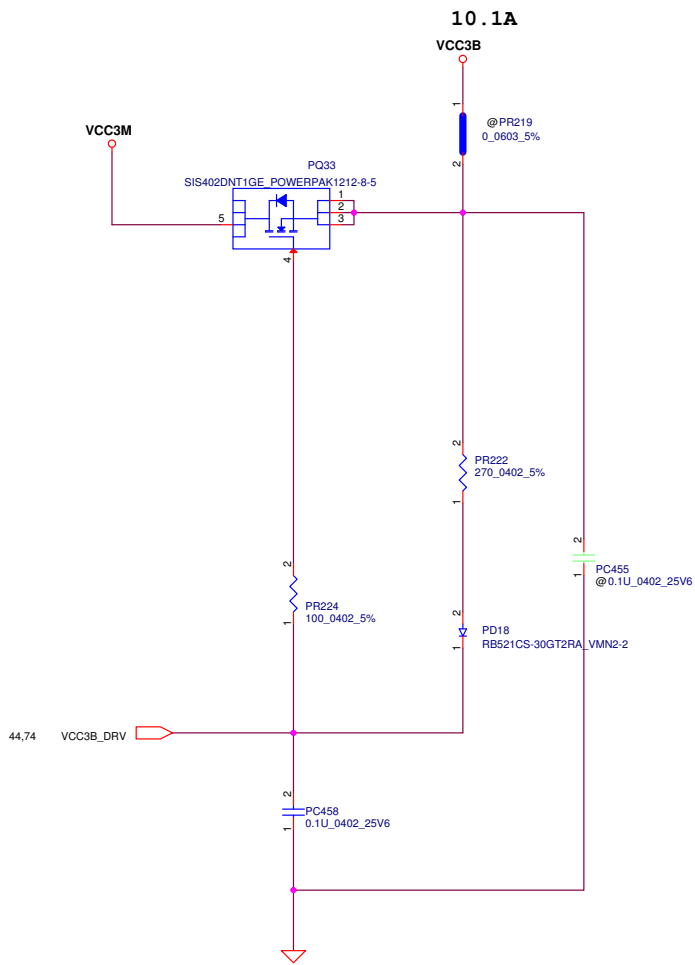


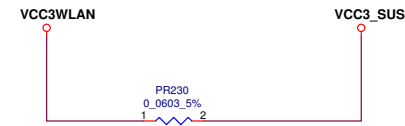
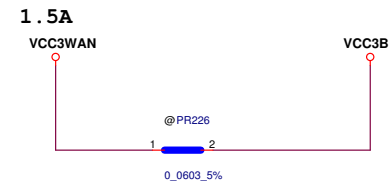
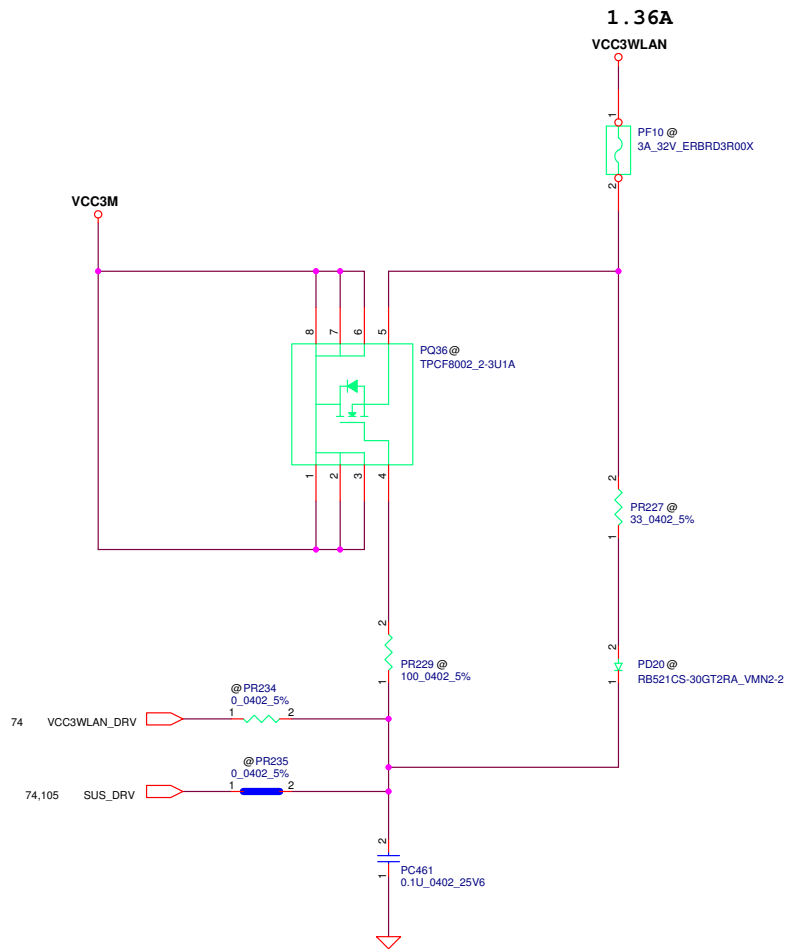
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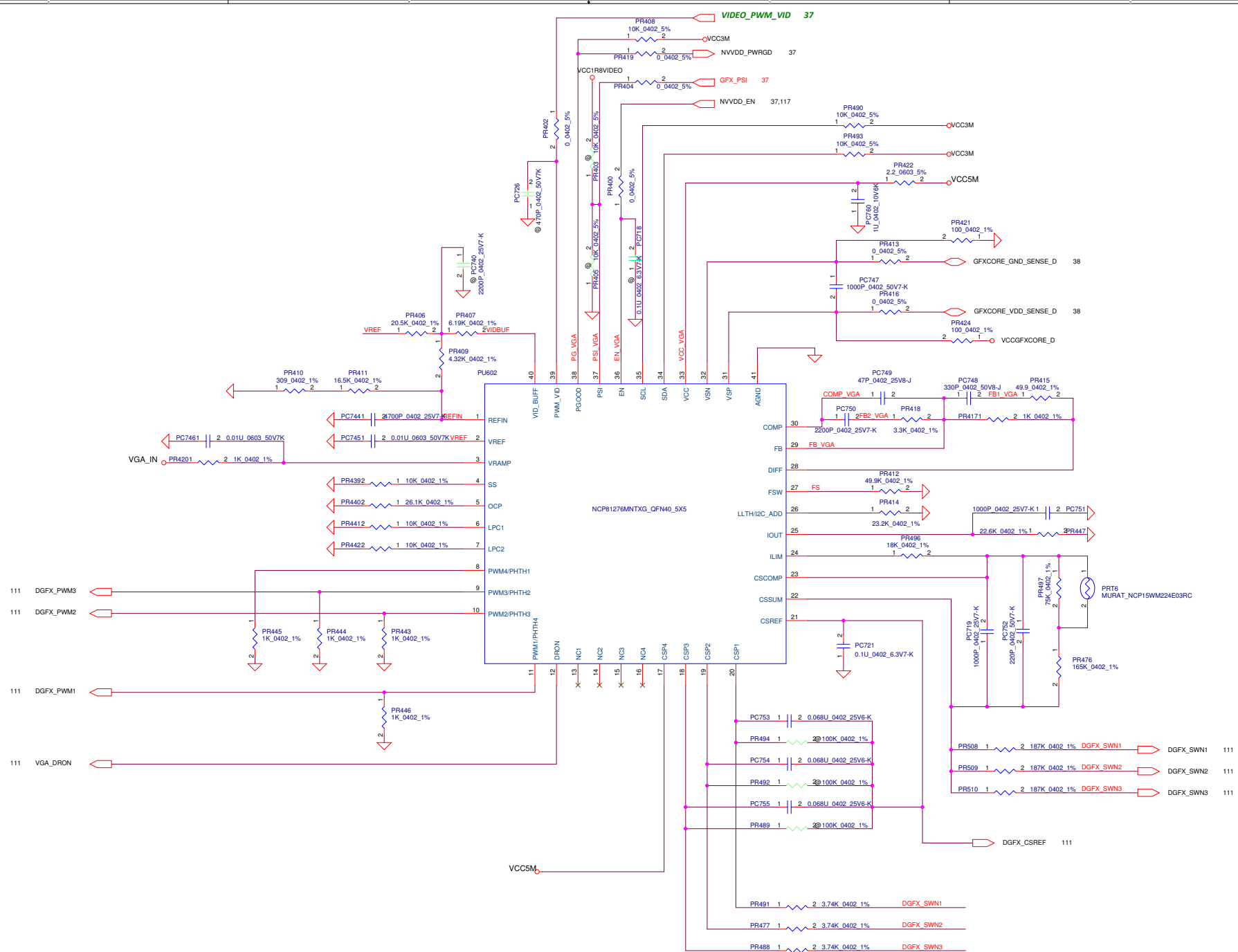


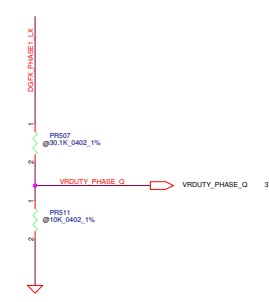
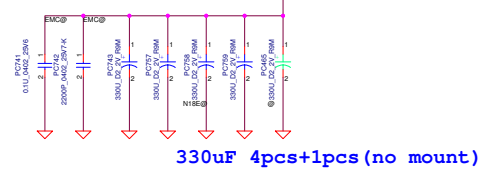
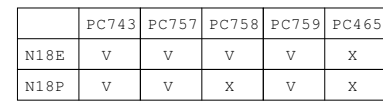
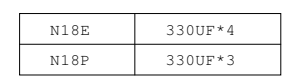




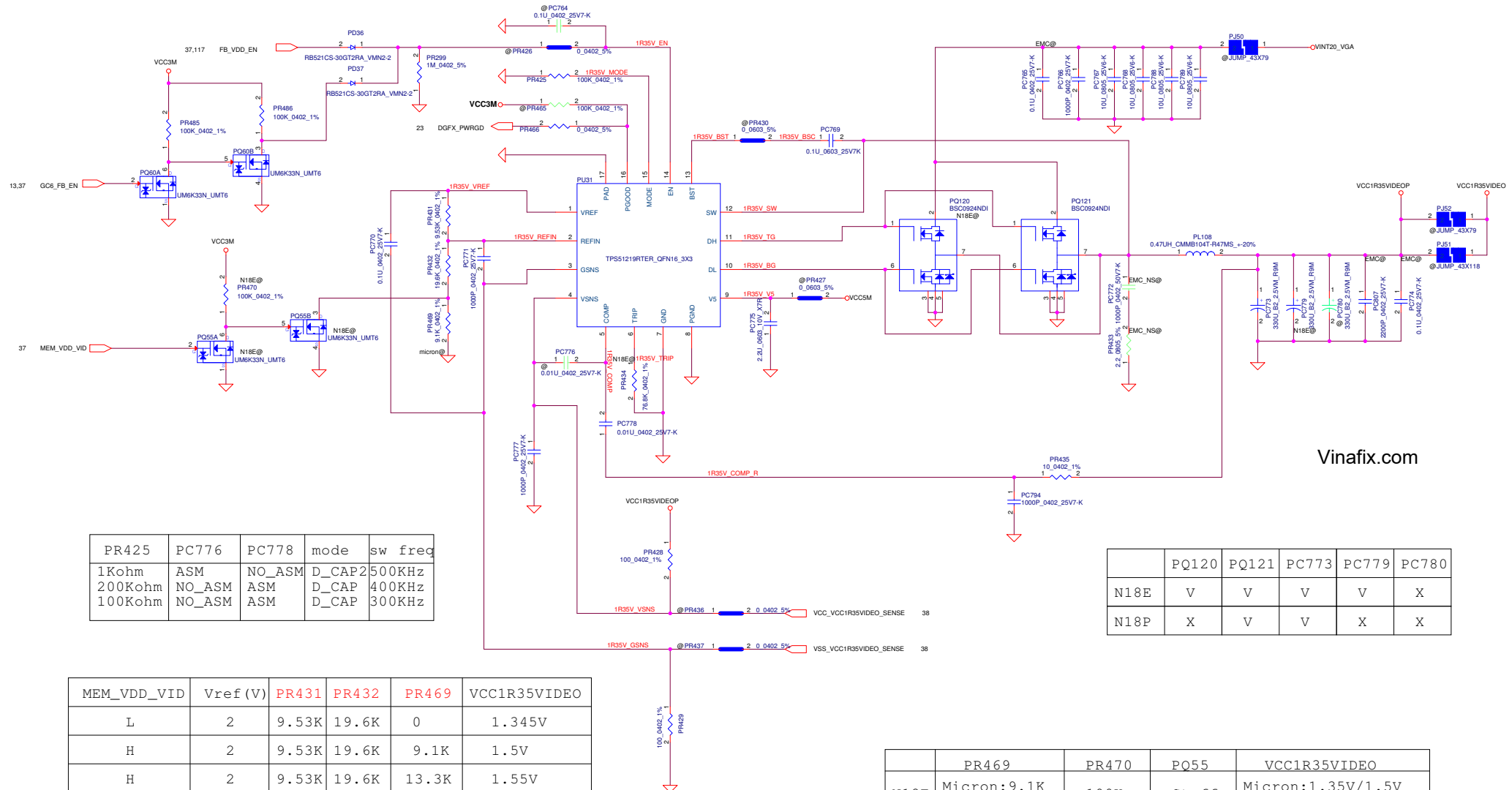
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LC Future Center Secret Data		Project Name	
		<i>Walter-3</i>	
		Rev 0.4	Title BLANK
Date: Monday, June 25, 2018		Sheet 109 of 117	





	EDP-continue	EDP-Peak	OCP
N18E	20A	33A	40A
N18P	10A	13A	17A



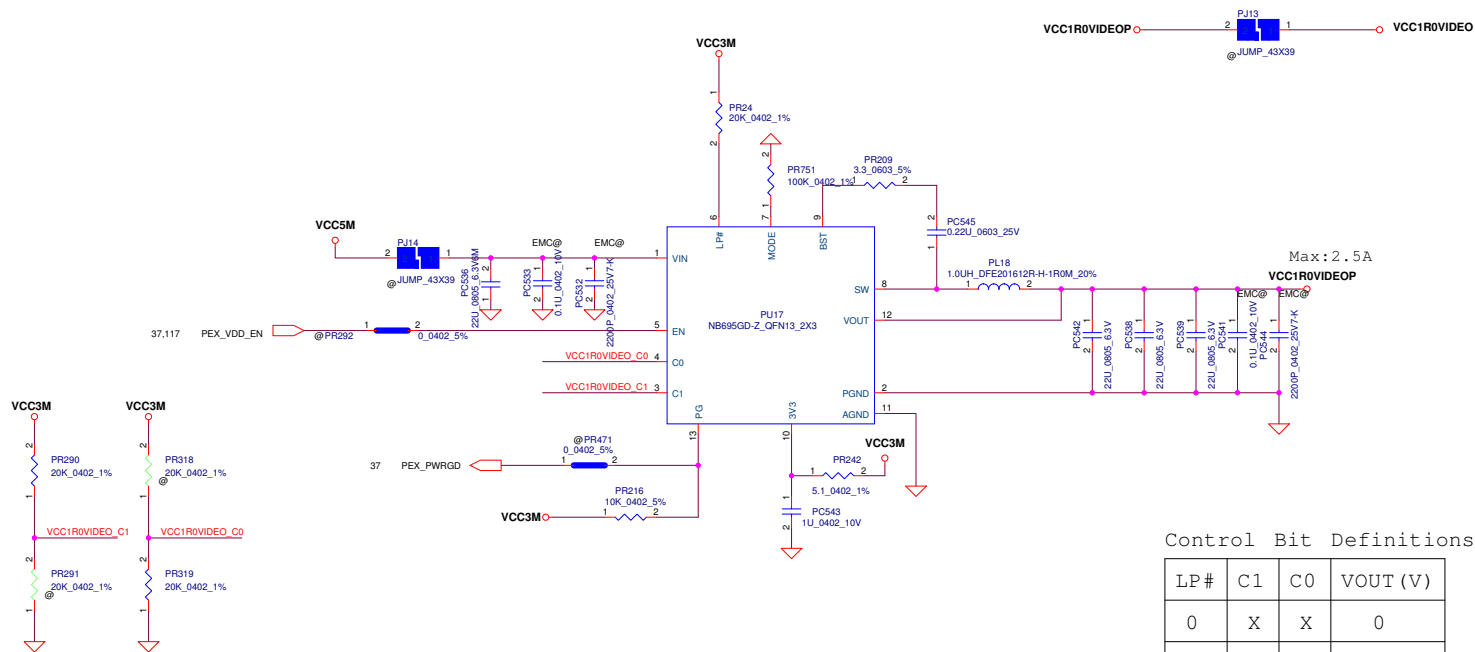
PR425	PC776	PC778	mode	sw freq
1Kohm	ASM	NO_ASM	D_CAP2	500KHz
200Kohm	NO_ASM	ASM	D_CAP	400KHz
100Kohm	NO_ASM	ASM	D_CAP	300KHz

	PQ120	PQ121	PC773	PC779	PC780
N18E	V	V	V	V	X
N18P	X	V	V	X	X

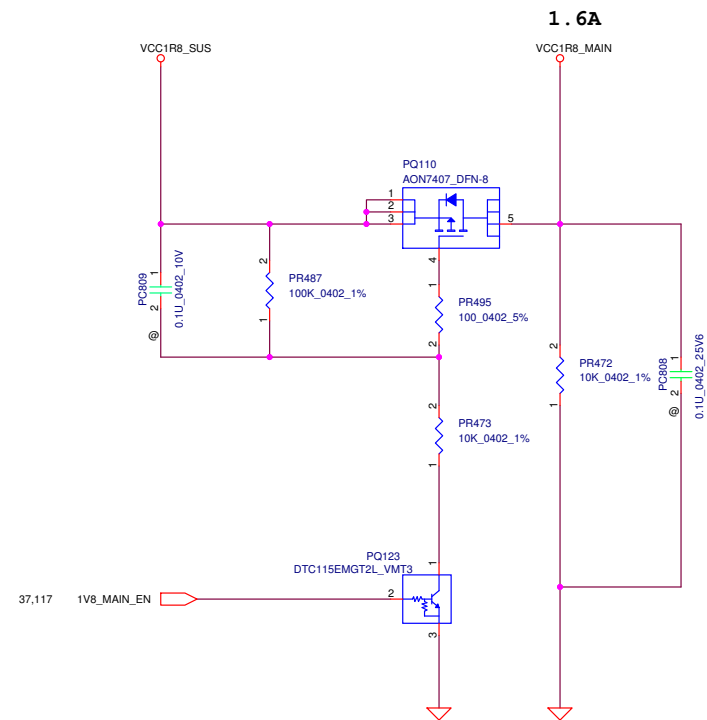
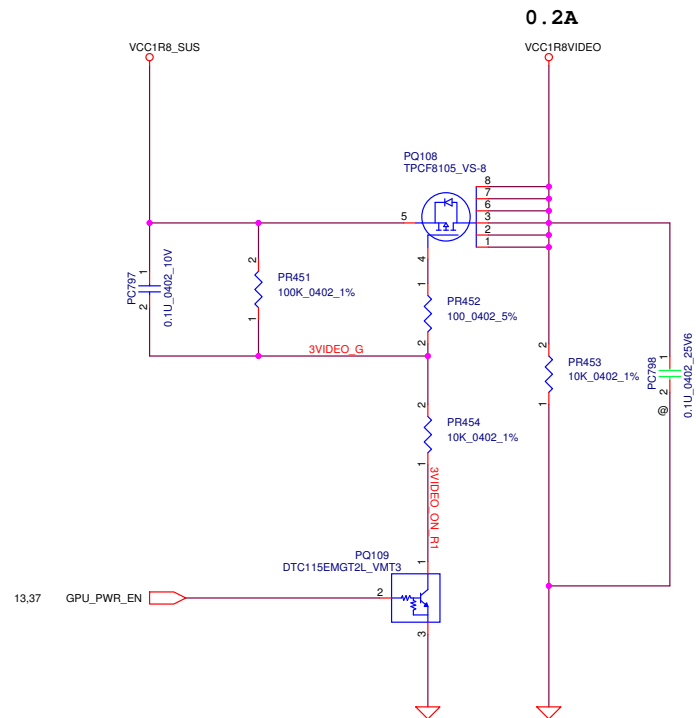
MEM_VDD_VID	Vref (V)	PR431	PR432	PR469	VCC1R35VIDEO
L	2	9.53K	19.6K	0	1.345V
H	2	9.53K	19.6K	9.1K	1.5V
H	2	9.53K	19.6K	13.3K	1.55V

Samsung VRAM	1.35V/1.55V
Micron VRAM	1.35V/1.5V

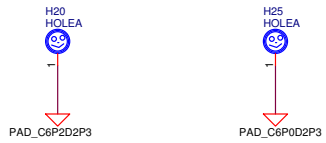
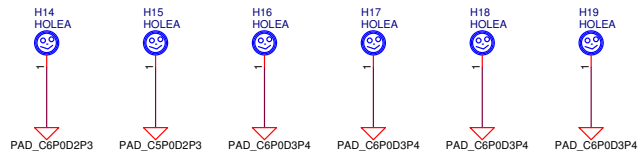
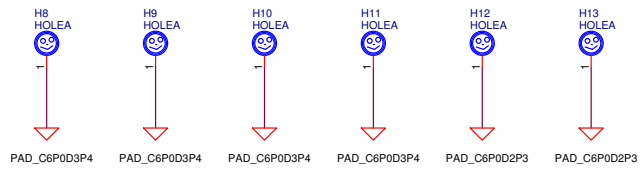
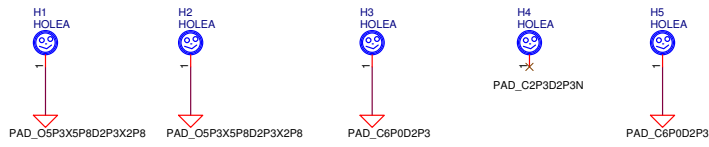
	PR469	PR470	PQ55	VCC1R35VIDEO
N18E	Micron:9.1K Samsung:13.3K	100K	Stuff	Micron:1.35V/1.5V Samsung:1.35V/1.55V
N18P	0ohm	No Stuff	No Stuff	1.35V



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Walter Unique



PCB Fedical Mark PAD

